

REVISION RECORD			
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I2C	Function	I2C Spec. [1]	Budgeted Timing	I2C Slave Address (7-bit mode)
I2C-0 * [2]	SW charger	400 Kbps		bq25896 / SW charger I2C address: 0X6B (Write:0xD6, Read:0xD7)
	LCM Gate Driver	400 Kbps		NT50338 / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
	Buck-boost	400 Kbps		FAN49101 / Buck-boost I2C address: 0X70 (Write:0xE0, Read:0xE1)
	Flash LED Driver	400 Kbps		LM3643 / Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)
	Speaker Amp.	400 Kbps		MAX98928EWV-T / Speaker AMP I2C Address: 0x31 (Write:0x62, Read:0x63) when ADDR = GND. MAX98928EWV-T / Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69) when ADDR = VIO18.
	USB Type- C CC	400 Kbps		FUSB302 / USB Type- C channel configure I2C Slave Address:0x22, write:0x44, read:0x45 or FUSB302 / USB Type- C channel configure I2C Slave Address:0x23, write:0x46, read:0x47
	MHL	400 Kbps		SI8348 / CI2CA Low-MHL I2C Address =0x39/3D/4D/64/48/60.(Write:0x72/7A/9A/C8/92/C0, Read:0x73/7B/9B/C9/93/C1)
I2C-1 * [2]	M Sensor	400 Kbps		AK09912 / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)
	A+Gyro Sensor	400 Kbps	Yes.	ICM-20645 / A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Baro Sensor	400 Kbps		BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	RGB / PS Sensor	400 Kbps		CM36558 / ALPS + UV I2C address: 0X51 (Write:0xA2, Read:0xA3)
	Humidity Sensor	400 Kbps		HTS221 / Humidity I2C address: 0X5F (Write:0xBE, Read:0xBF)
I2C-2	Rear camera	400 Kbps	Yes.	OV23850 / Rear camera I2C address: 0X36 (Write:0x6C, Read:0x6D) if SID = low. OV23850 / Rear camera I2C address: 0X10 (Write:0x20, Read:0x21) if SID = high.
	Rear camera's AF	400 Kbps		LC898212XD-SH / AF driver I2C address: 0X72 (Write:0xE4 Read:0xE5)
I2C-3	2nd front camera	400 Kbps	Yes.	S5K5E2 / Rear camera I2C address: 0X10 (Write:0x20, Read:0x21); It can be changed by register[7:11] of addr 0x0107.
	Front camera	400 Kbps	Yes.	S5K3M2XXM3 / Front camera I2C address:0X2D (Write:0x5A, Read:0x5B);
	Front camera's AF	400 Kbps	Yes.	DW9714A / AF driver I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-4	CTP	400 Kbps	Yes.	GT1511 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0X14 (Write:0x28, Read:0x29)
I2C-5	NFC	1.3 Mbps	Yes.	MT6605 / NFC I2C address: 0X28 (Write:0x50, Read:0x51)
I2C-6	VPROC buck	3.4 Mbps	Yes.	MT6313 / 2-2Phase Buck I2C address: 0X6B (Write:0xD6, Read:0xD7)
I2C-7	VGPU Buck	3.4 Mbps	Yes.	FAN53555 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)
Note 1: I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)				
Note 2: For MEMS sensor/sensor hub application, these I2C slave devices must be connected to I2C0 or I2C-1.				

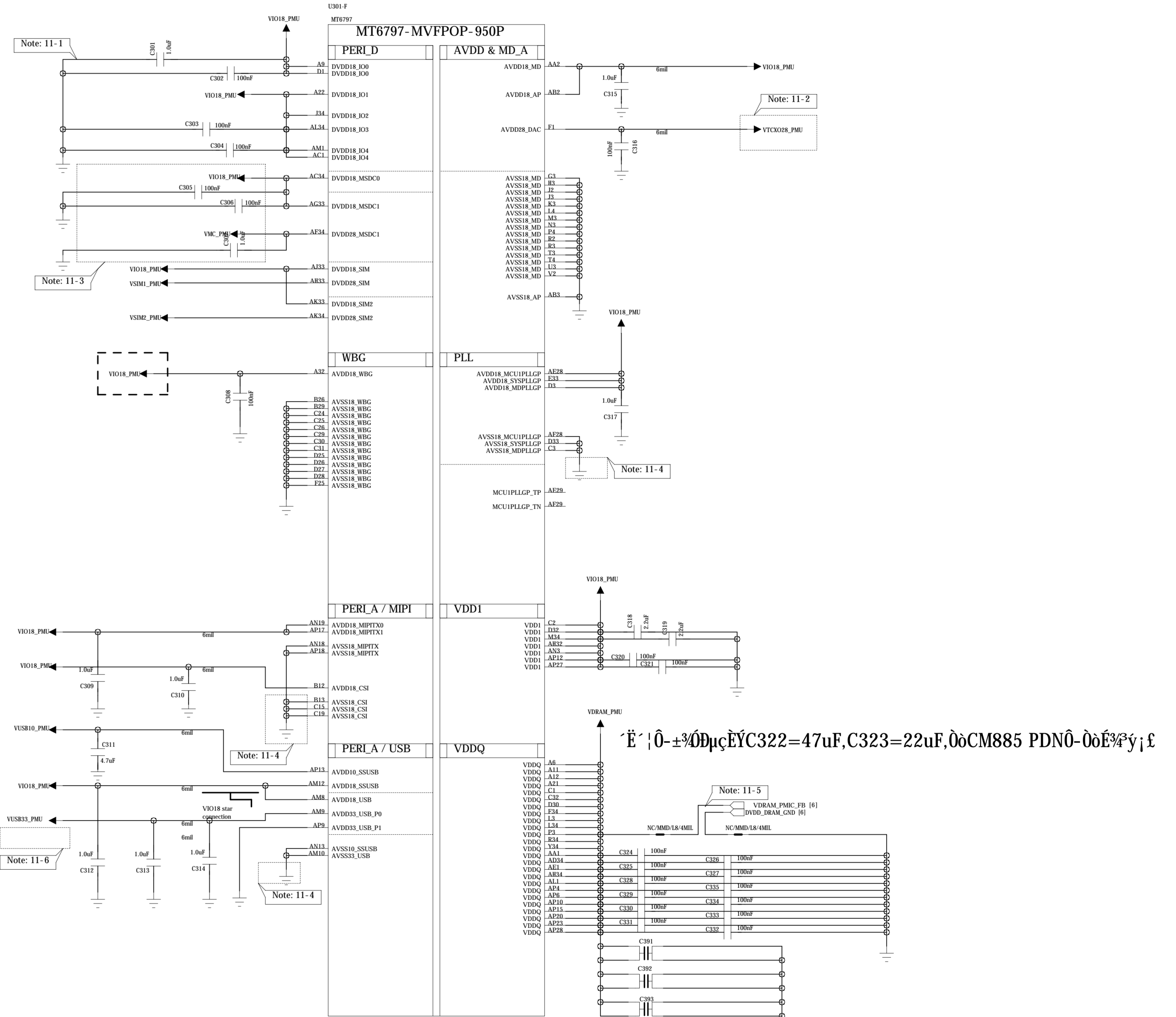
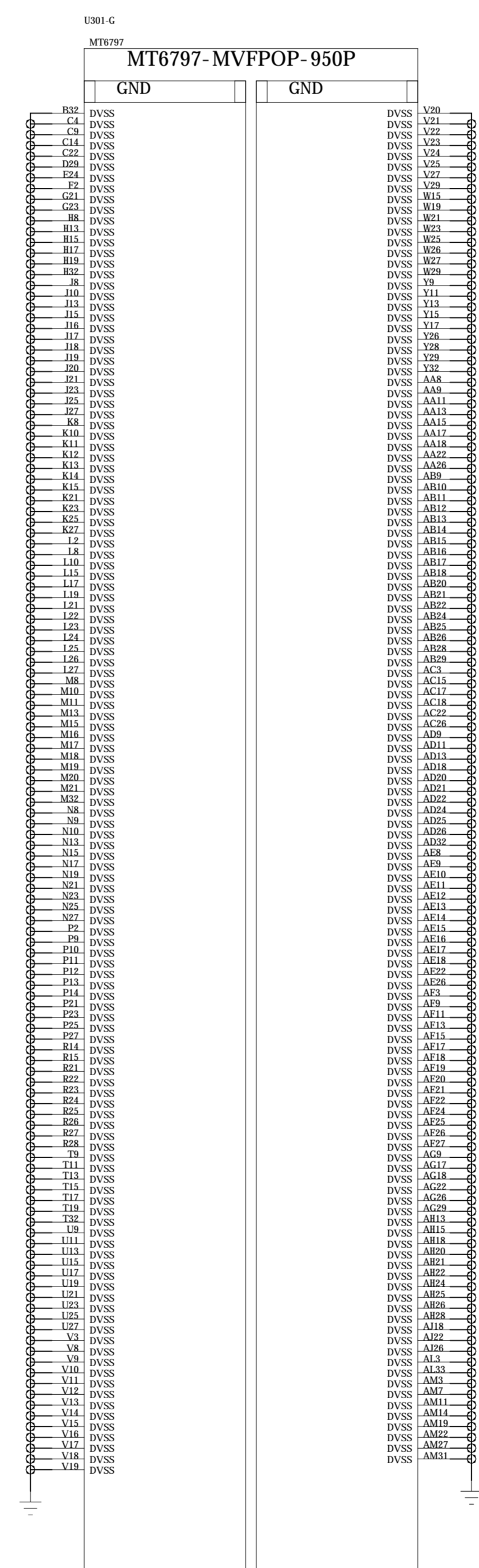
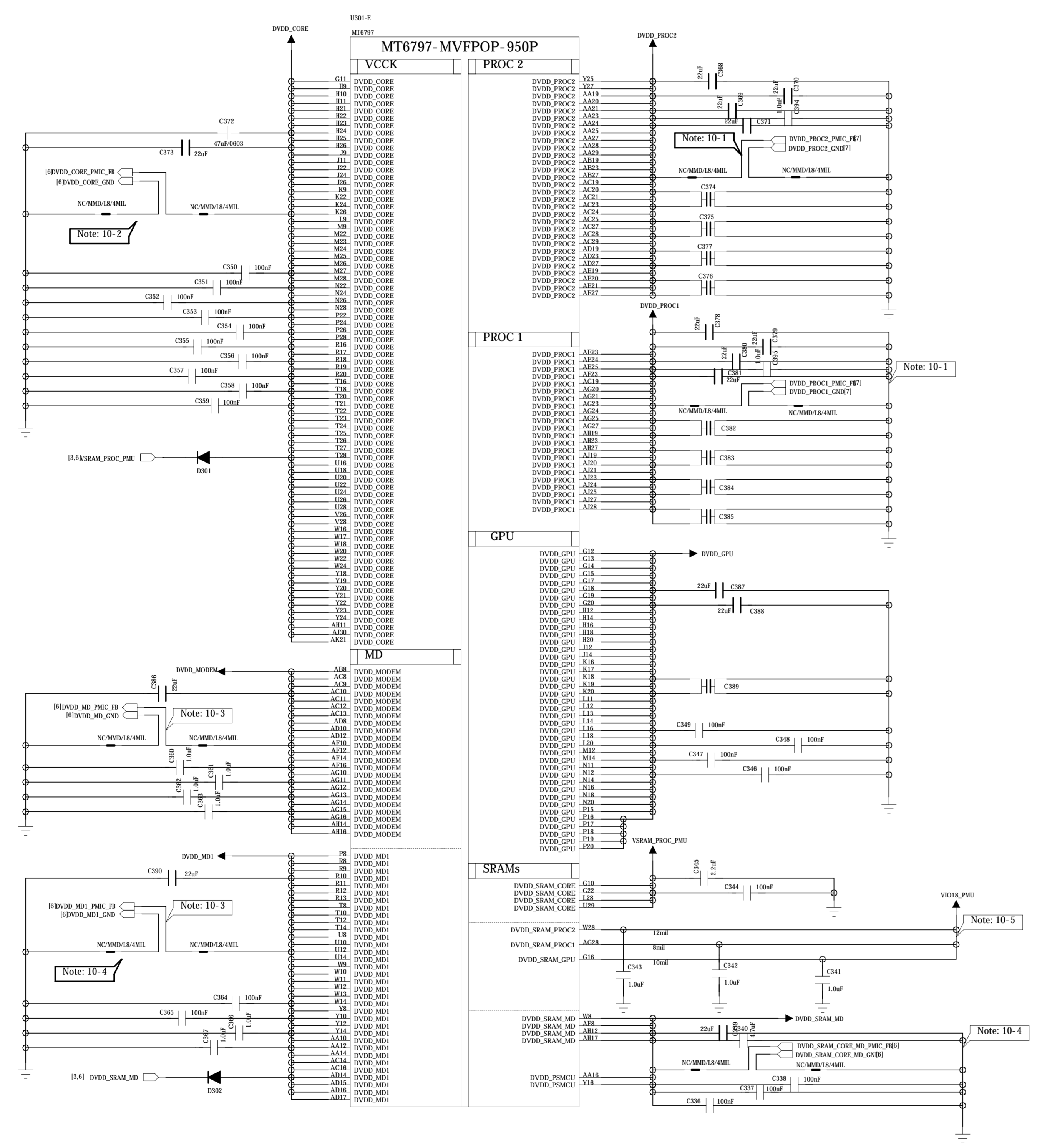
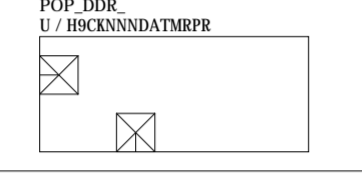
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Schematic design notice of "10_BB_POWER_1" page.

- Note 10-1:
- Note 10-2:
- Note 10-3: Differential pairs of buck's remote sense must be placed at PCB back side right beneath MT6797 chip.
- Note 10-4:
- Note 10-5: For PCB layout, the star connection should be implemented in the MT6351's VI018 output.

The purpose of this symbol is used for including POP LPDDR3 in BOM.

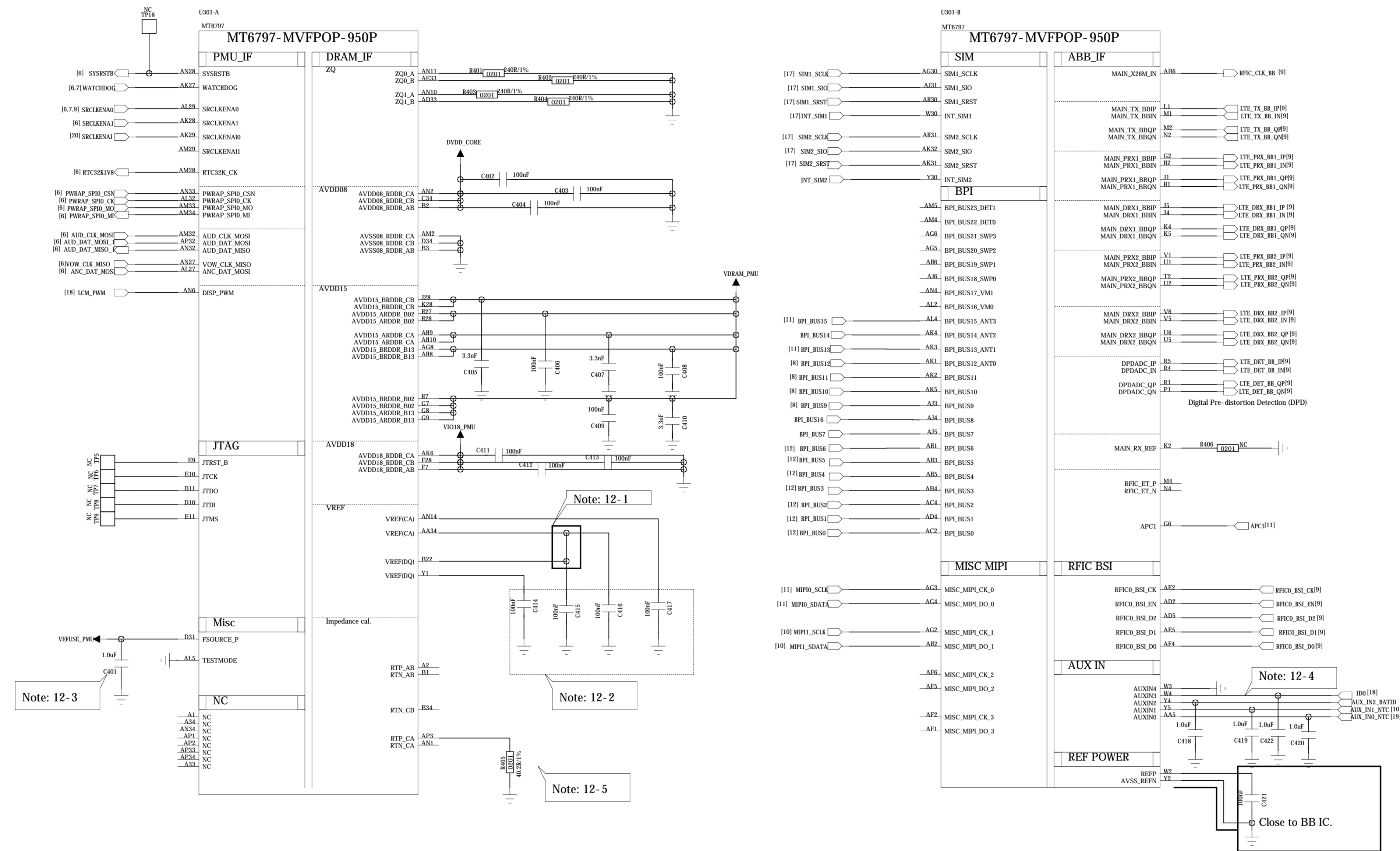


Schematic design notice of "11_BB_POWER" page.

- Note 11-1: Reserve 1uF capacitor in VCC1800 for MIL.
- Note 11-2: AVDD28_DAC (F1 ball) must be powered by "VTCX028_PMU".
- Note 11-3:
- Note 11-4: The placement of power/de-coupling capacitors of DVDD18_MSDC0/1 & DVDD28_MSDC1 should be placed in the farthest power plane from MT6351 point of view.
- Note 11-5: Differential pair of VDRAM_PMU remote sense should be placed in the farthest power plane from MT6351 point of view.
- Note 11-6: Connect AVDD33_USB_P1 to "VUSB33_PMU" for USB application; Connect AVDD33_USB_P1 to "VSM1_PMU" for IC-USB / Smart card application.

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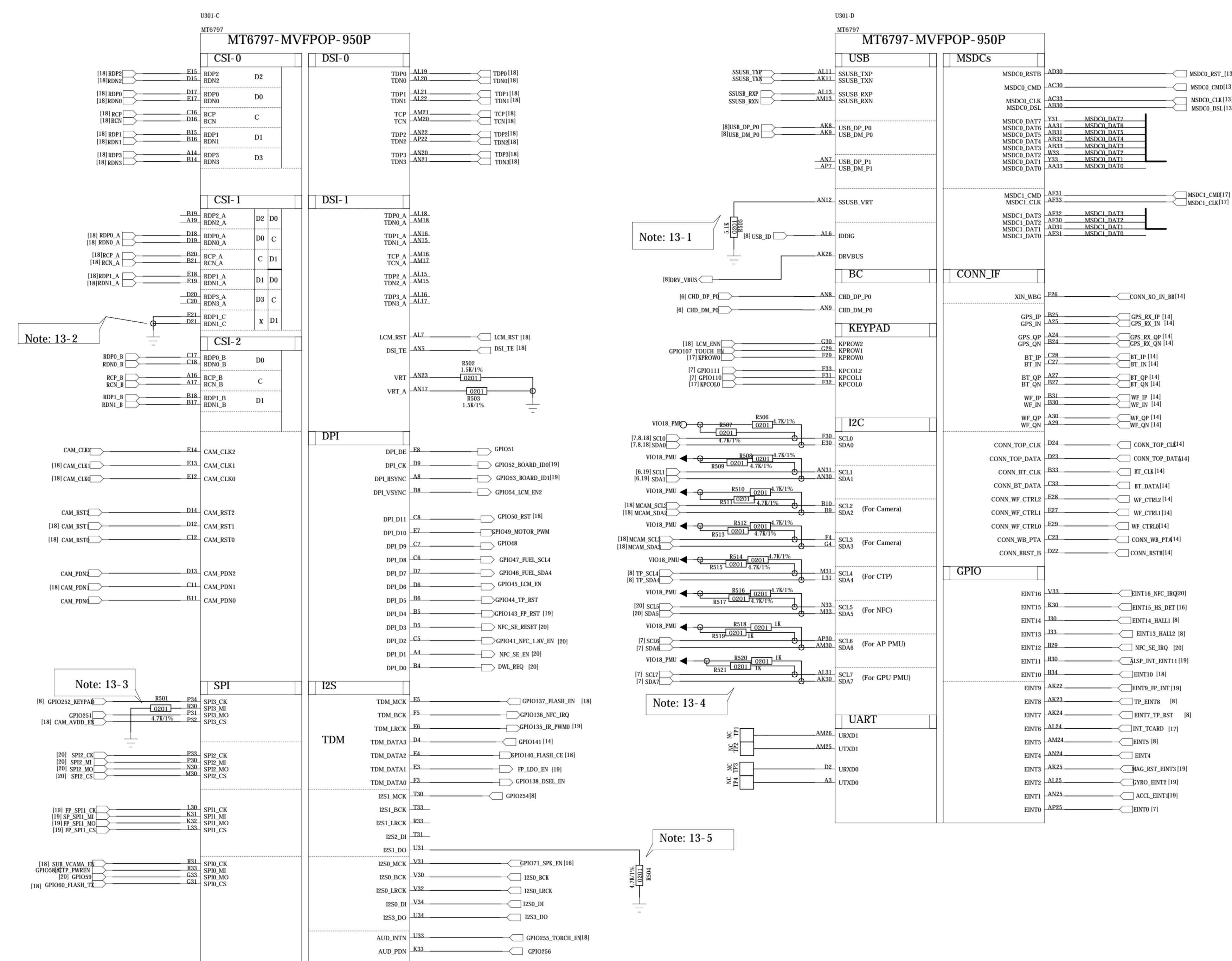
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- Schematic design notice of "11_BB_11" page.
- Note 12-1: The DRAM's VREFCA(AA34 ball) must connect to VREF(DQ)(B22 ball).
 - Note 12-2: The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible.
 - Note 12-3: Apply 1.8V to FSOURCE_P (D31) for eFuse programming.
 - Note 12-4: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.
 - Note 12-5: For impedance calibration of DDRPHY

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Schematic design notice of "12_BB_2" page.

Note 13-1: Default resistor of "SSUSB_VRT" can be NC if internal USB VRT is applied.

Note 13-2: Connect the NC pins of CSI to GND

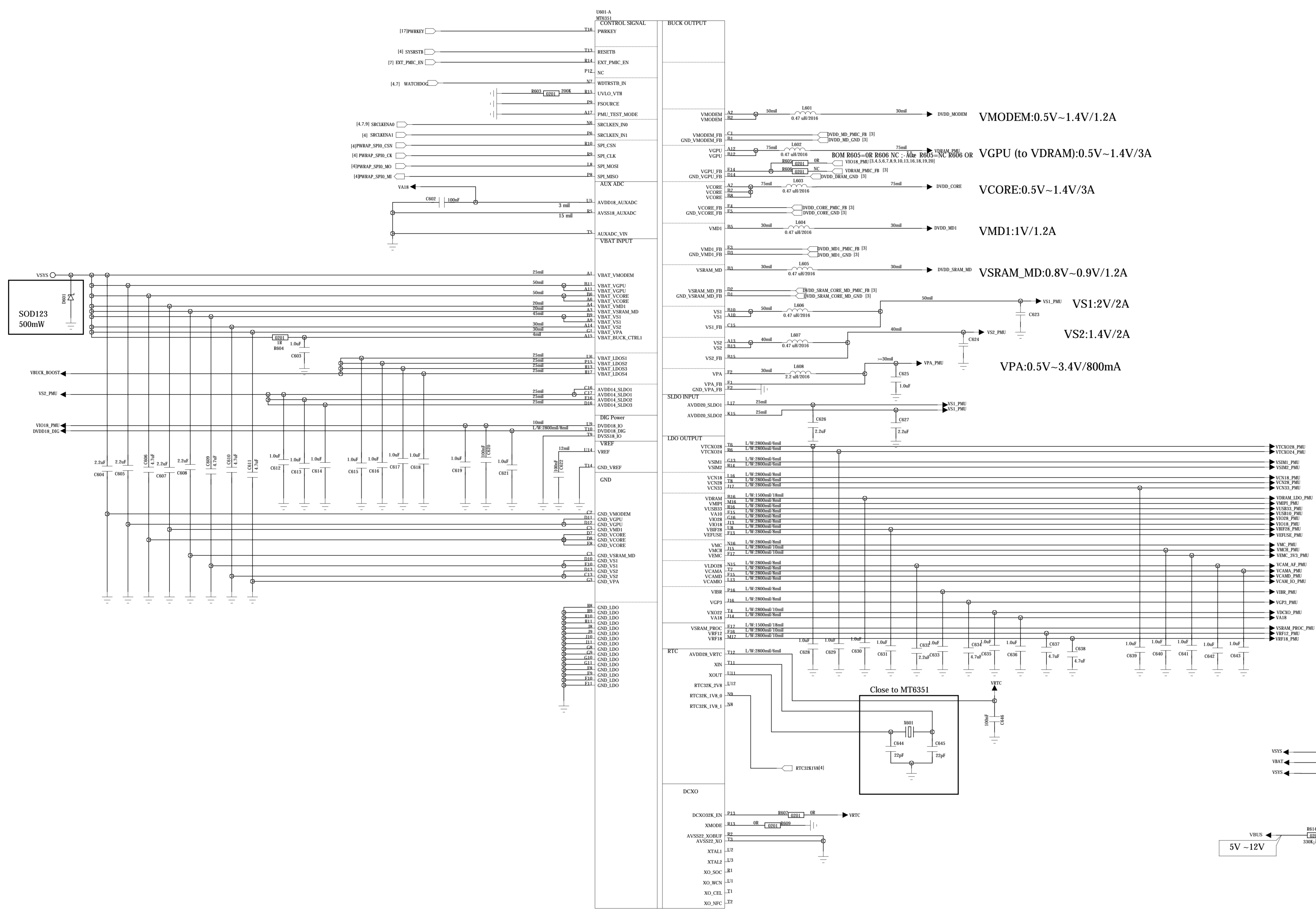
Note 13-3: The GPIO250 can't have external pull-up. "C2K DROP_ZONE" output indicator is not allow to have external pull-up.

Note 13-4: The I/O type of I2C6/7 is push-pull. External pull-up is required if I2C6/7 slave devices can only support open-drain.

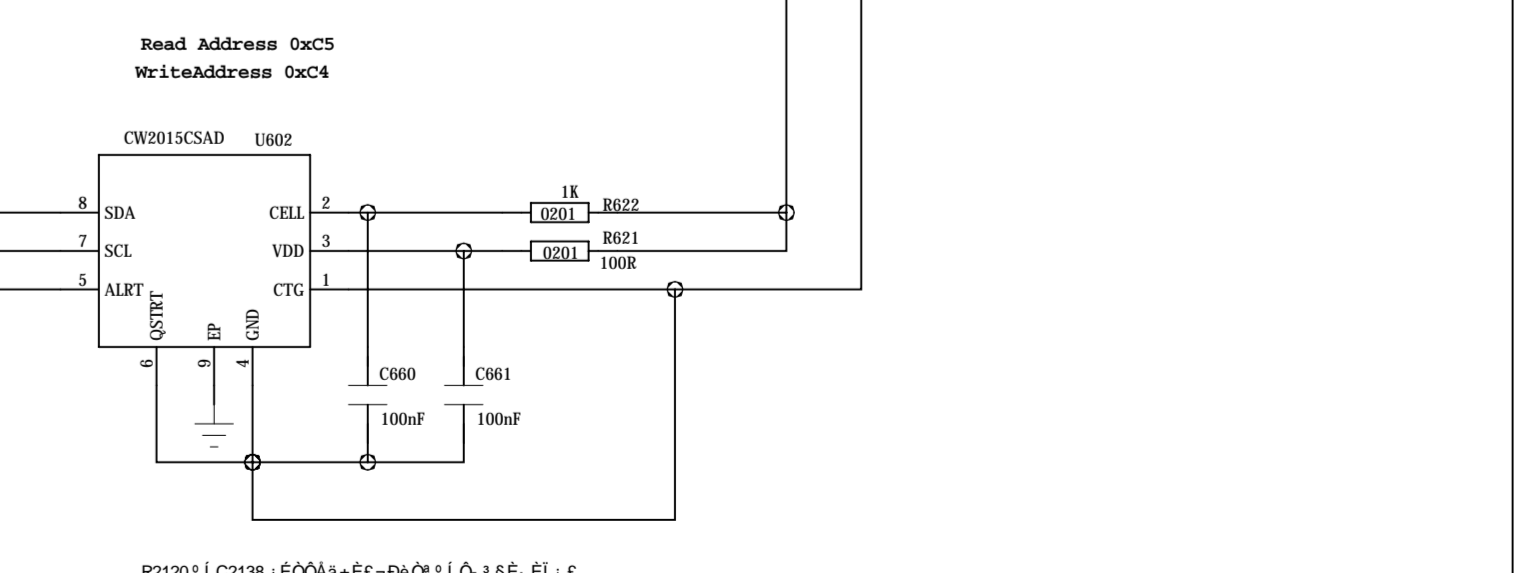
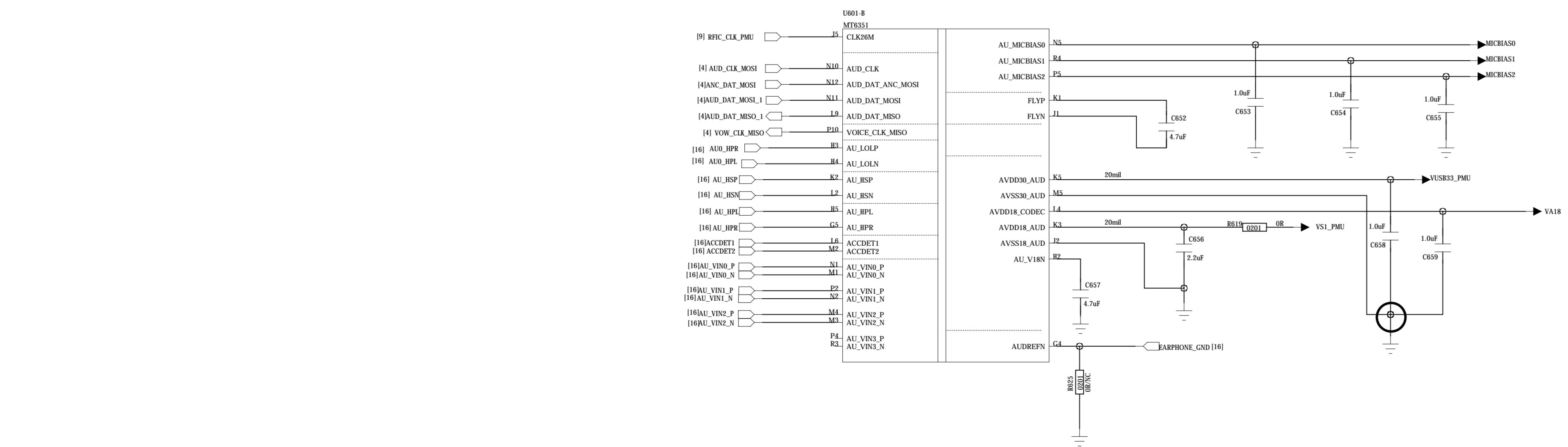
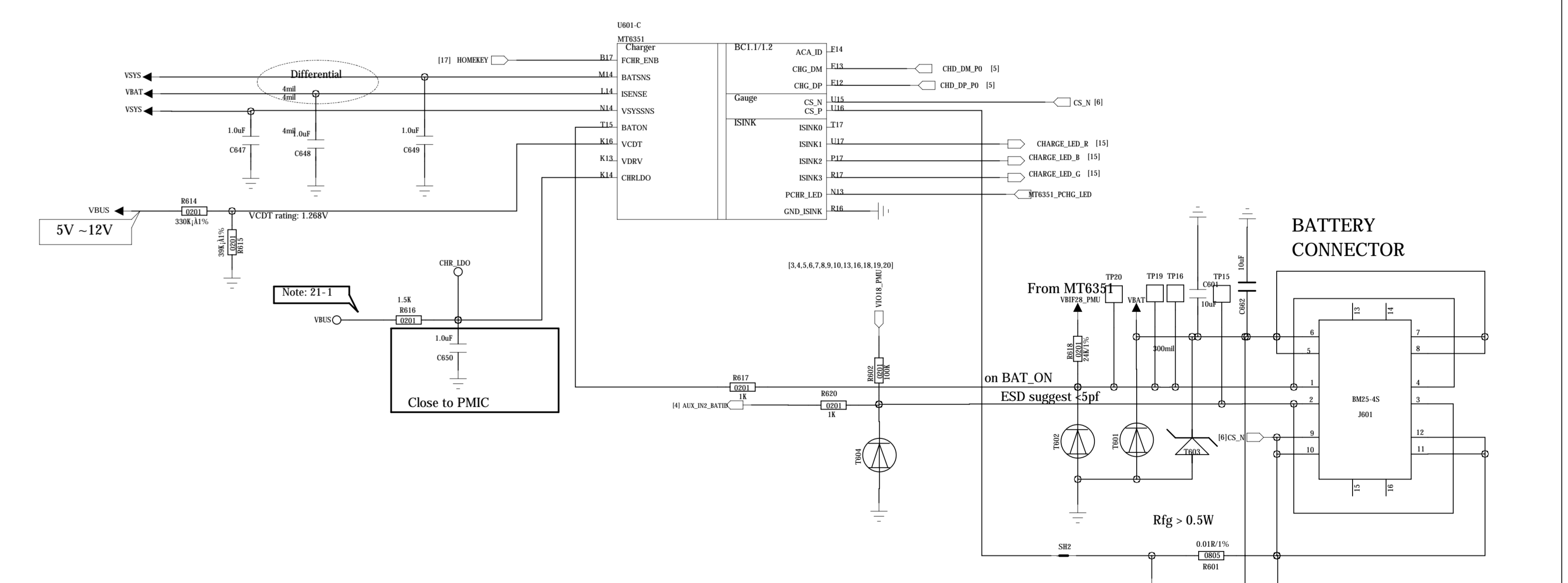
Note 13-5: The GPIO249 features I/O trap in system bootup that must be pulled down.

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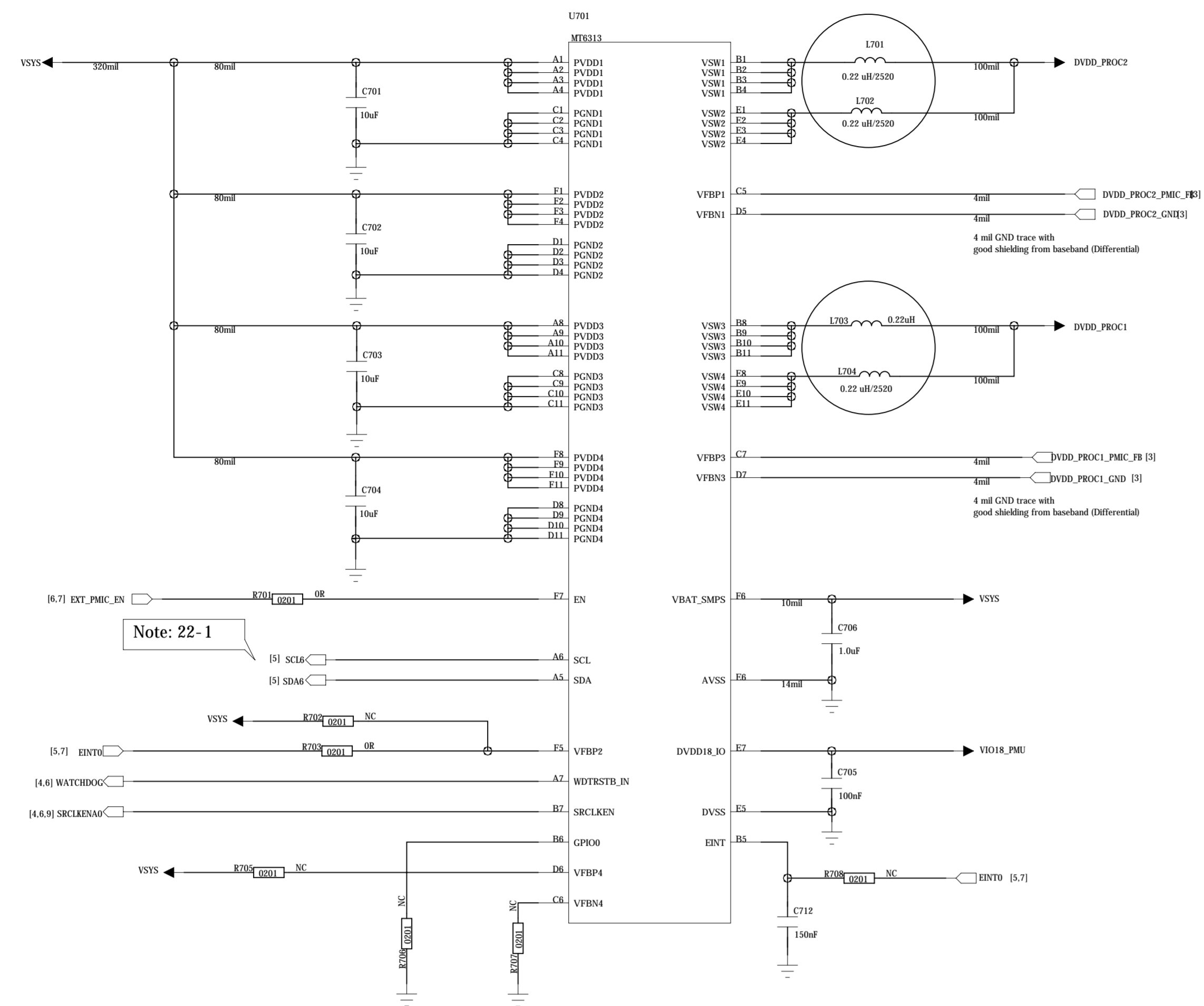
Schematic design notice of "21_POWER_MT6351_2" page.
 Note 21-1: Reserve 1.5K in order to give additional power to turn on charger LED driver while low battery.



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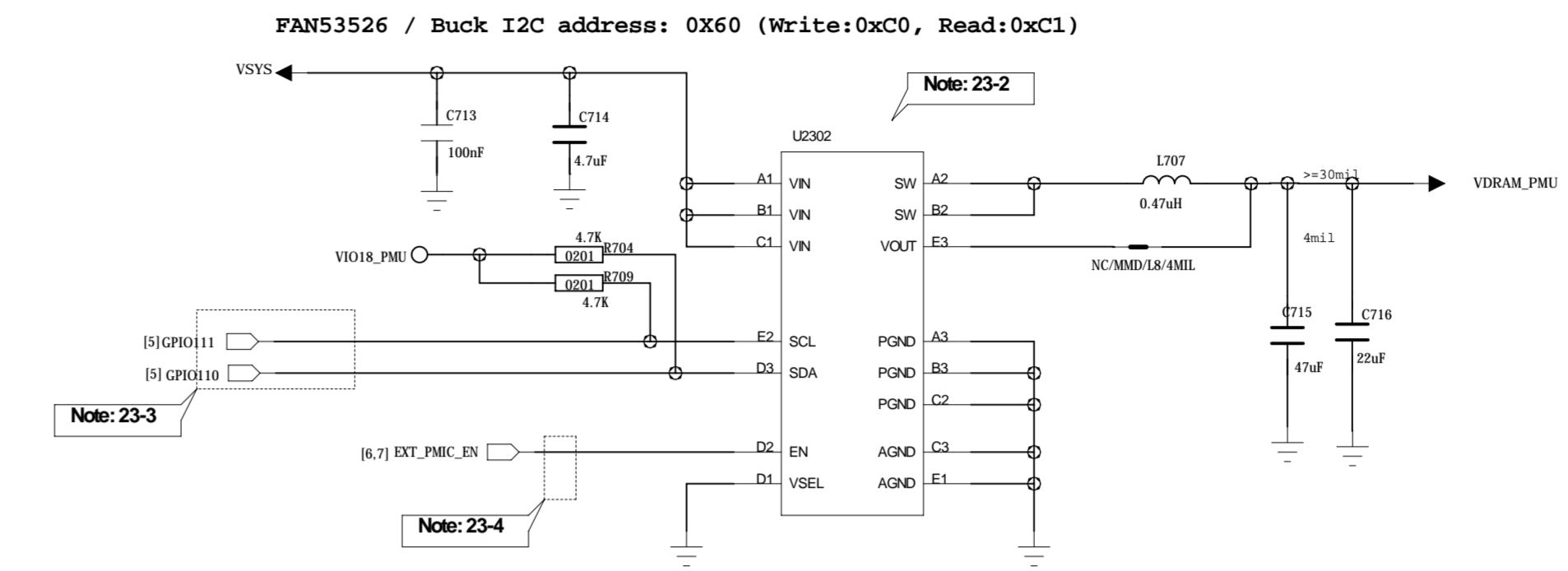
VPROC Buck



Schematic design notice of "22_POWER_2+2PHASE_BUCK" page.

Note 22-1: Buck EN is controlled by SRCLKEN0 or I2C

Buck for VDRAM



Schematic design notice of "23_POWER_VGPU_VM" page.

Note 23-2: BOM option to select MT6351's VGPU or 3rd party PMC as VDRAM (1.2V) power

	UZ302	PL2302	C2303	C2304	R2301	R2302
MT6351's VGPU as VDRAM	NC / DNI	NC / DNI	NC / DNI	NC / DNI	NC / DNI	NC / DNI
3rd party PMC as VDRAM	FAN53526	0.47uF	0.1uF	4.7uF	4.7K	4.7K

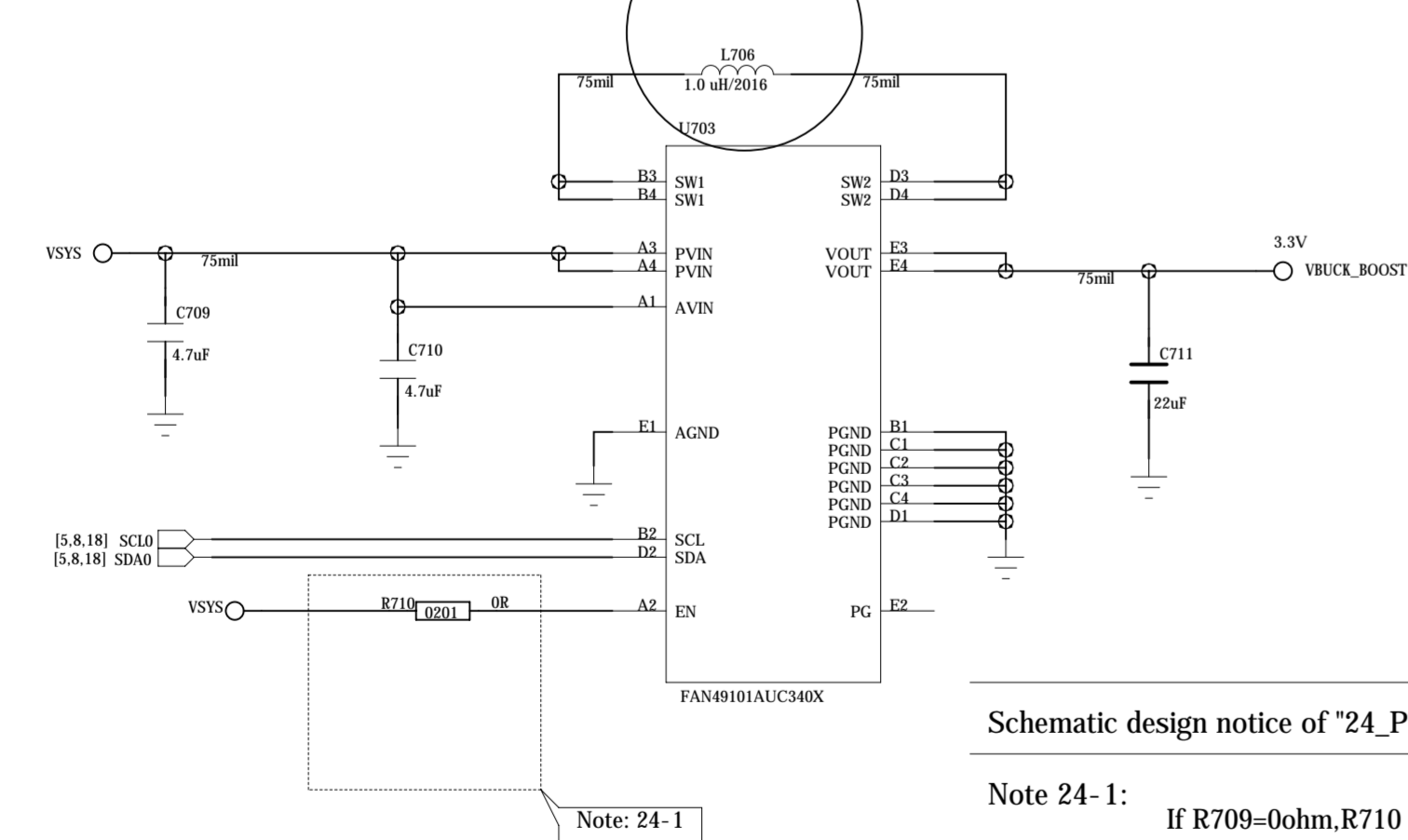
Note: NC / DNI = No connect / Do not install.

Note 23-3: Use pin muxed I2C-1 to control FAN53526 since its I2C base address is 0x60 same as VGPU and M-L.

Note 23-4: FAN53526's EN pin is driven by MT6351.

Companion Buck/Boost

FAN49101 / Buck-boost I2C address: 0X70 (Write:0xE0, Read:0xE1)

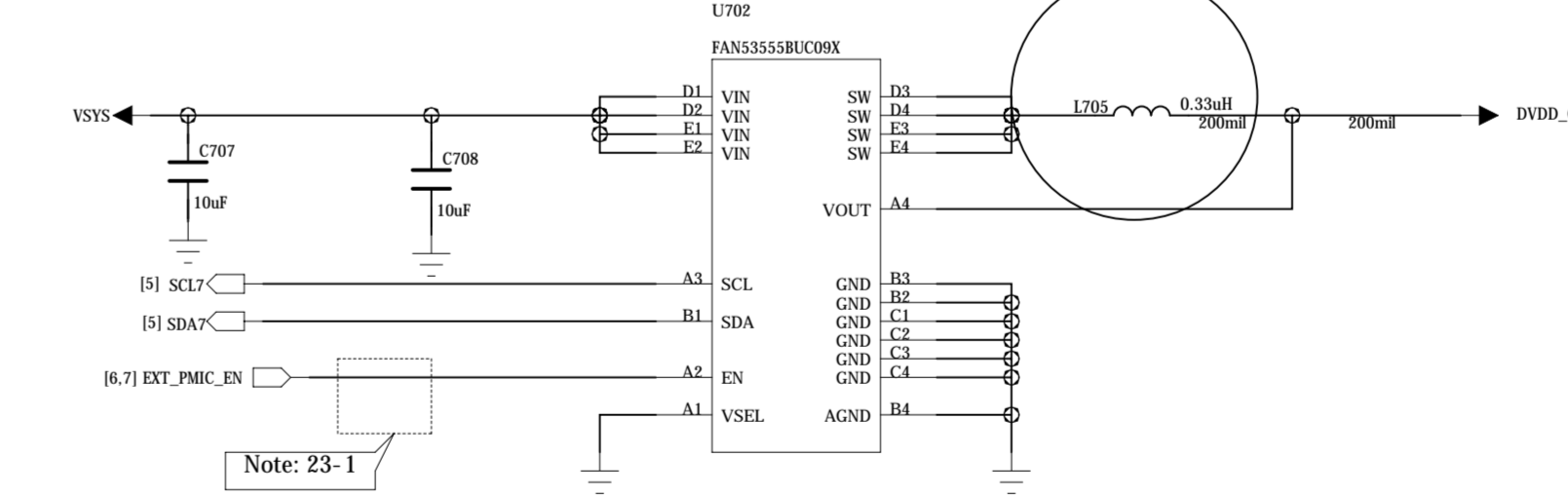


Schematic design notice of "24_POWER_THIRD-PARTY" page.

Note 24-1: If R709=0ohm,R710 NC,R5109=0ohm: MT6605 can't support card mode function when phone off (quick boot disable)
If R709=NC,R710=0ohm,R5109=0ohm: MT6605 can support card mode function when phone off(quick boot disable)

2-Phase Buck

FAN53555 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)



Schematic design notice of "23_POWER_VGPU" page.

Note 23-1: FAN53555's EN pin is driven by MT6351.

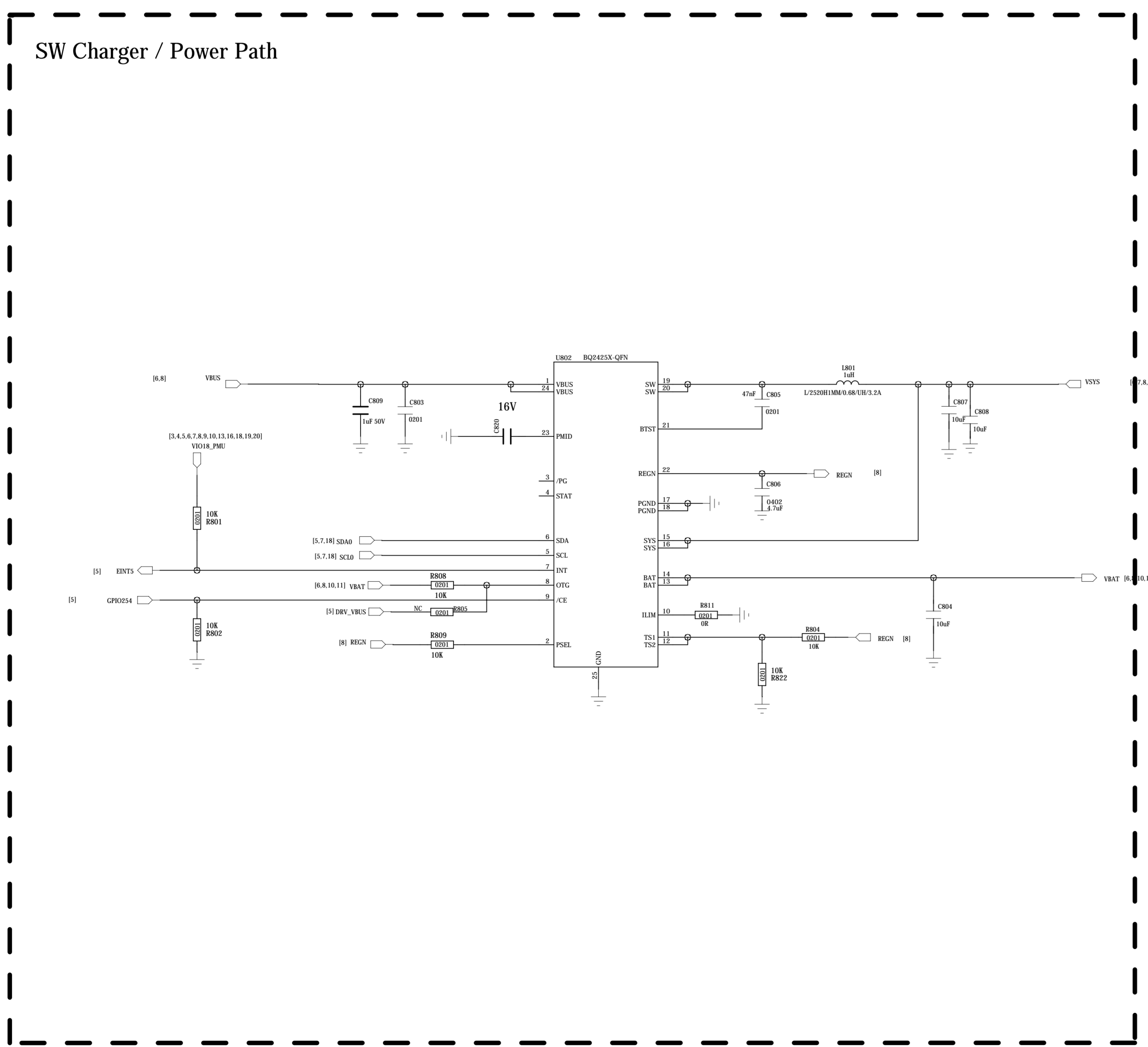
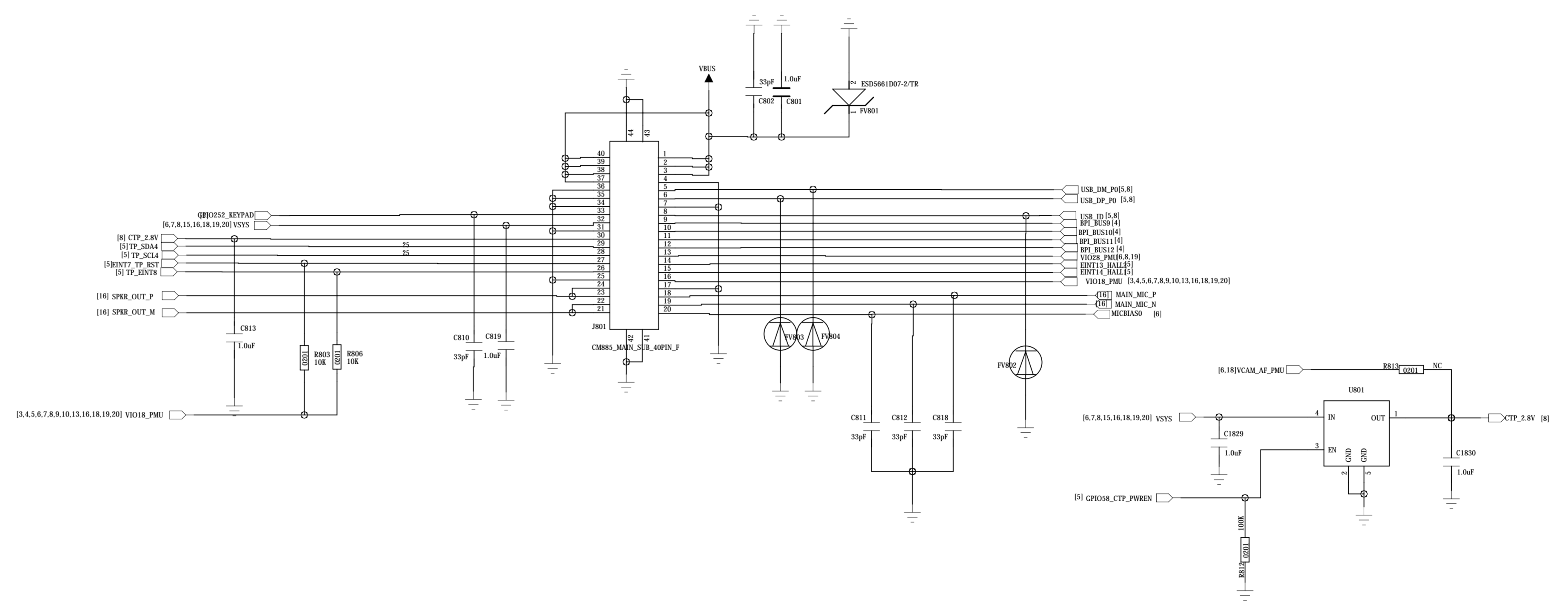
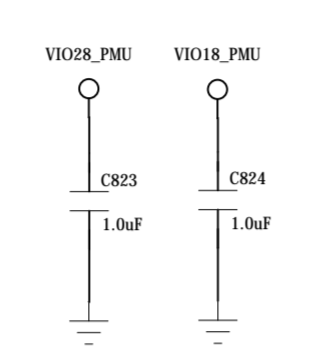
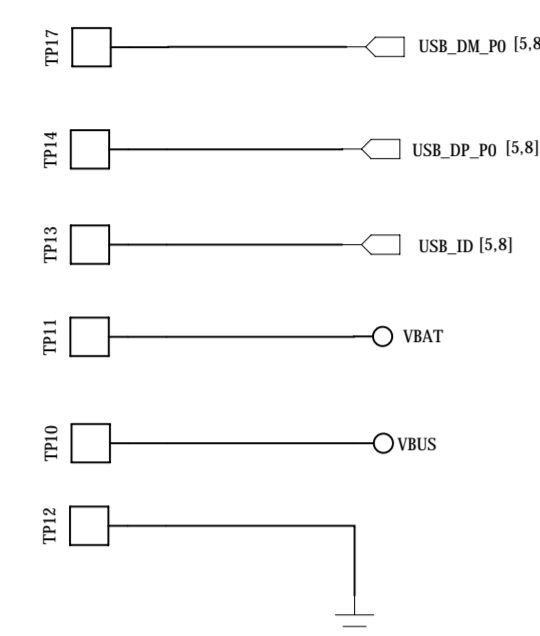
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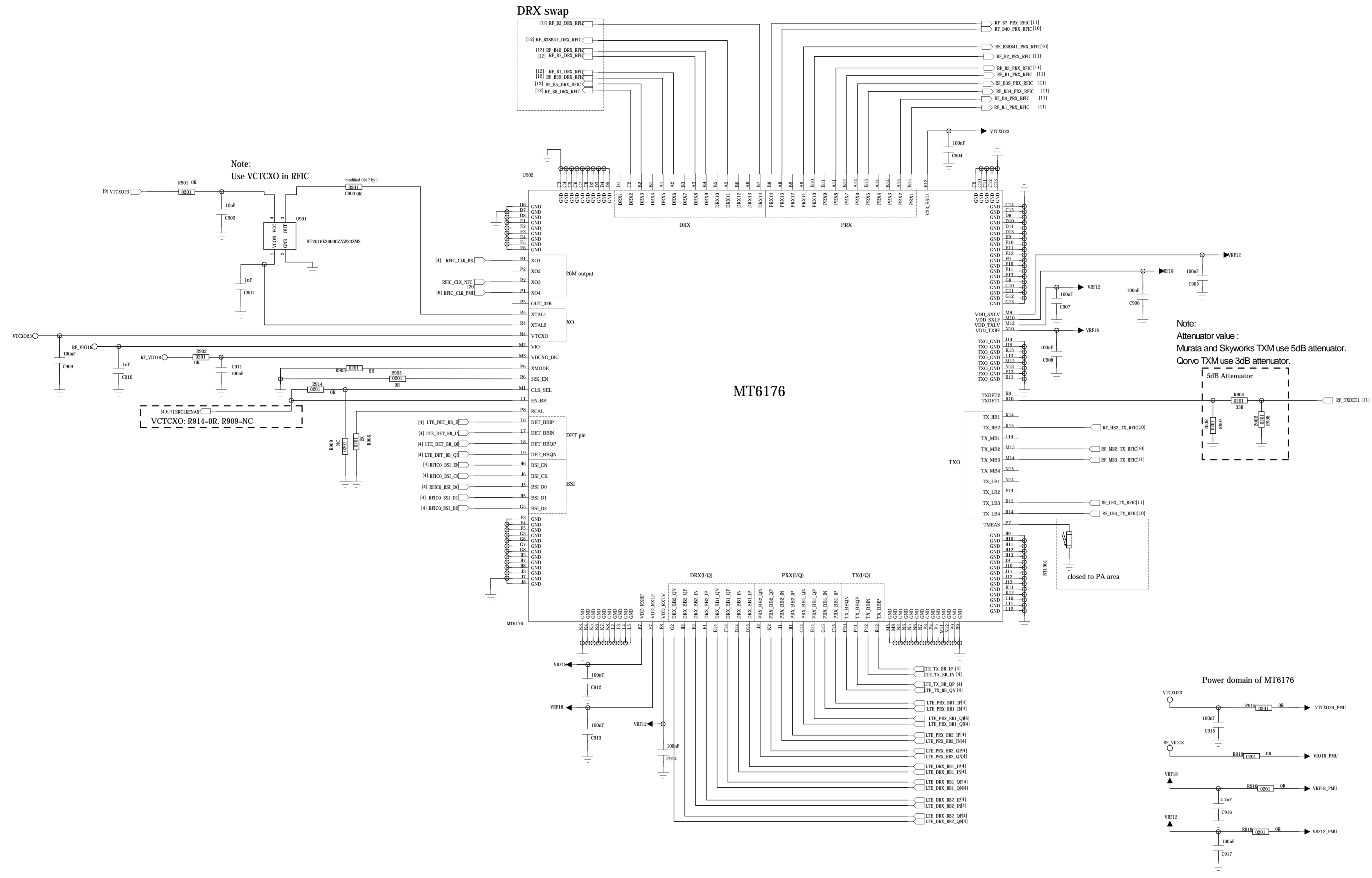
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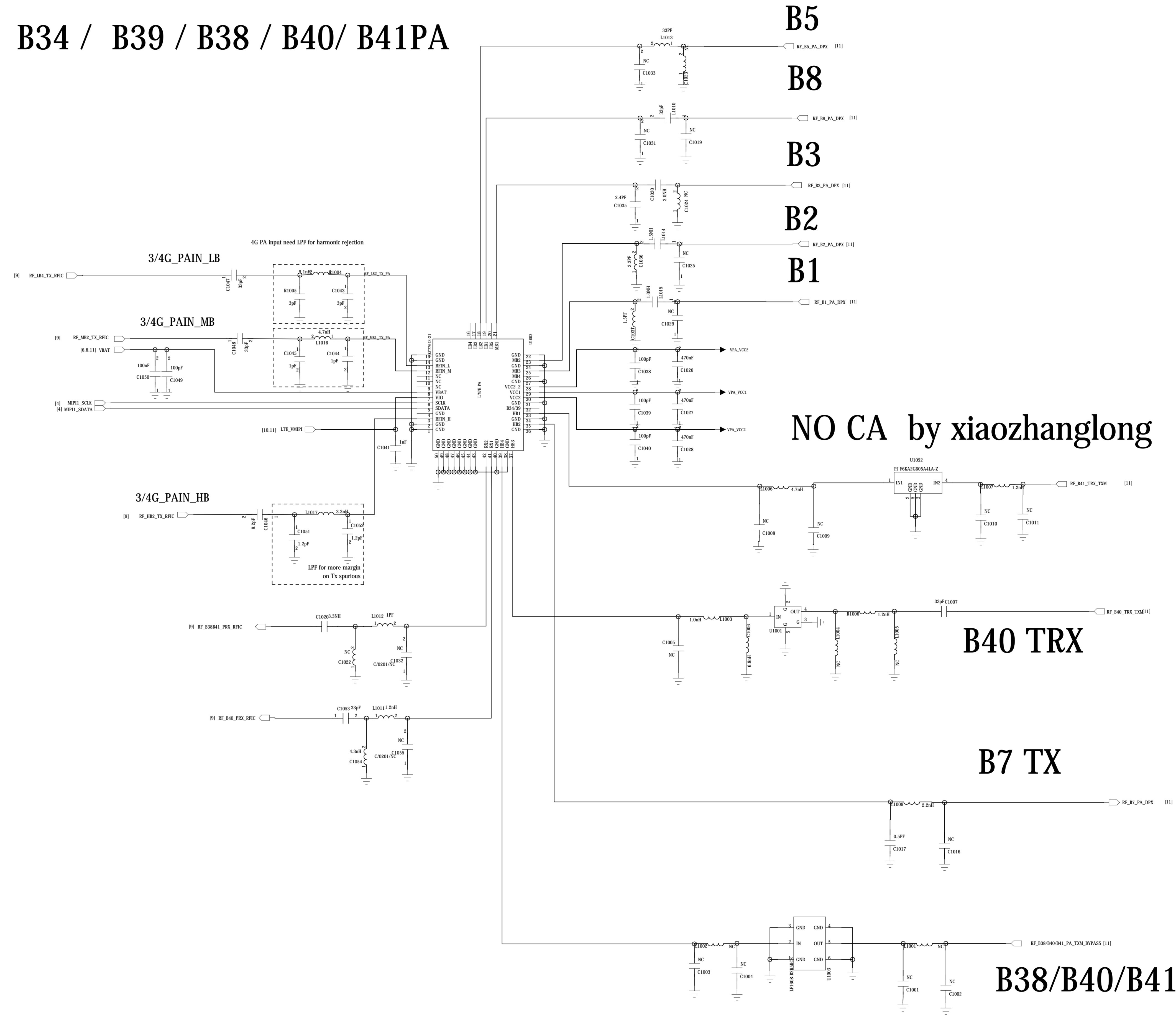
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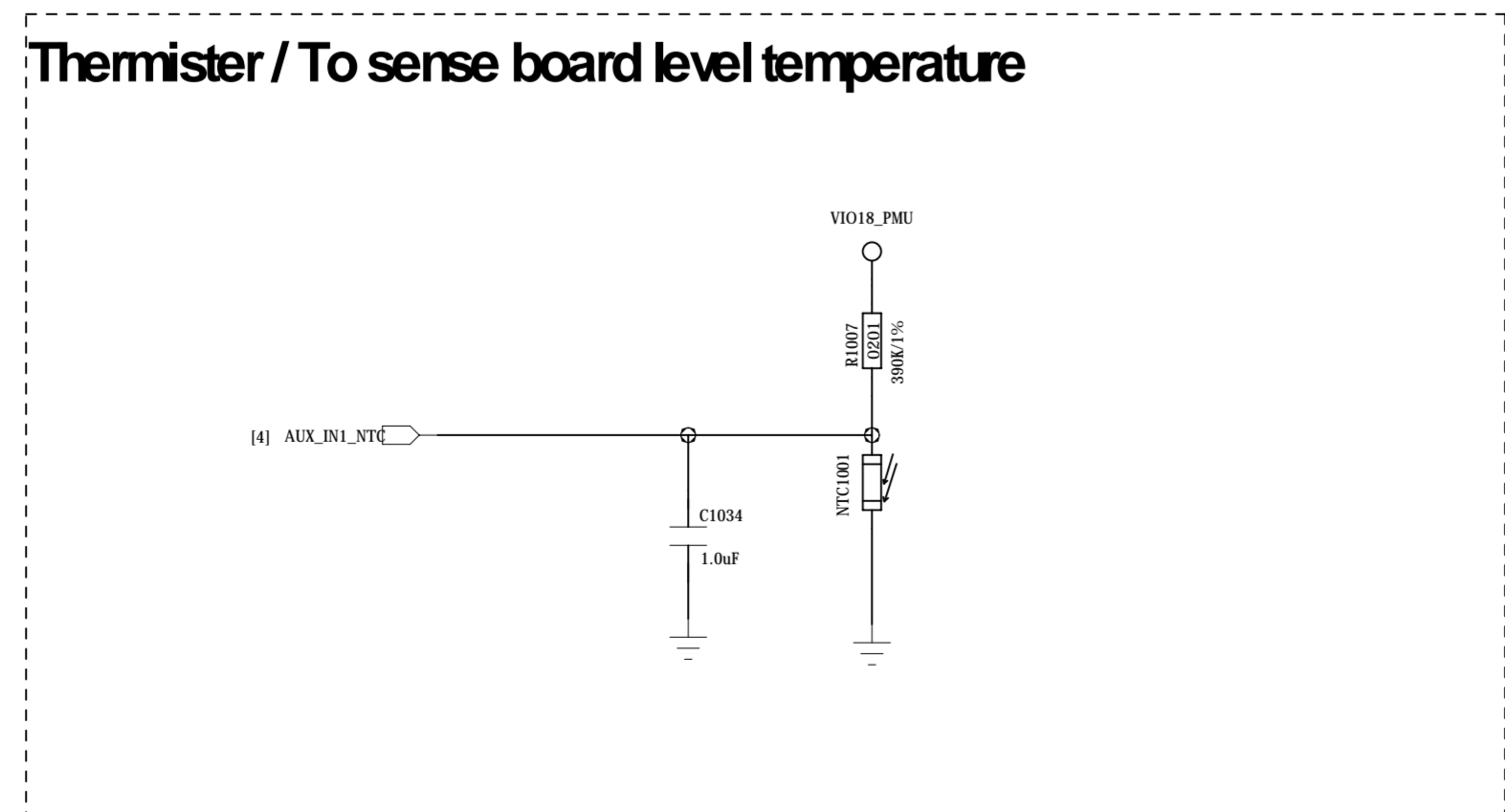
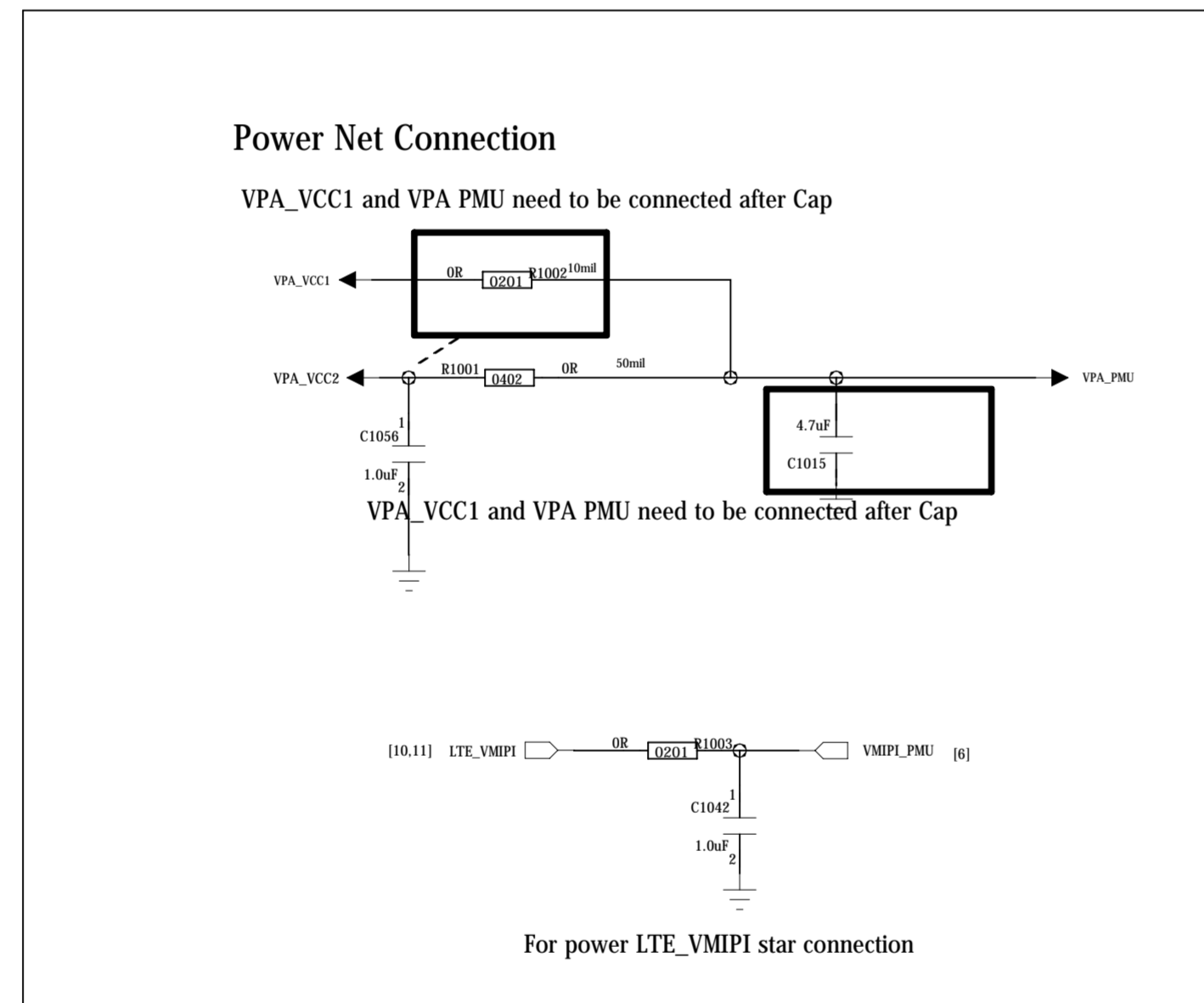
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B40 TRX

B7 TX

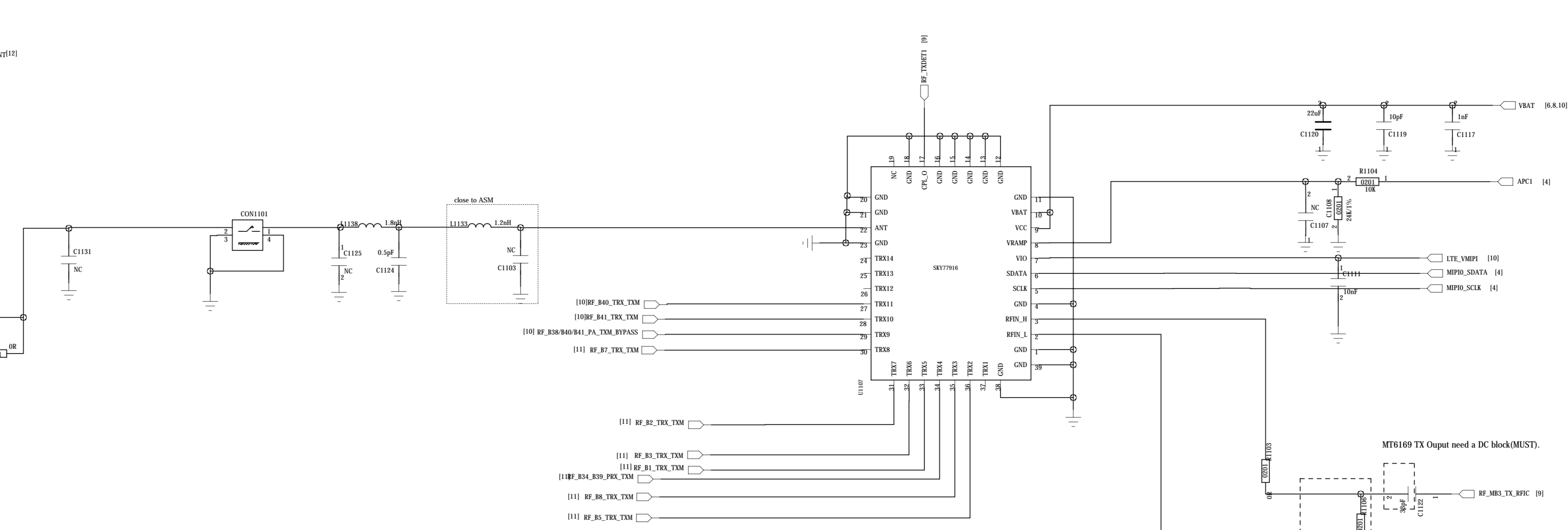
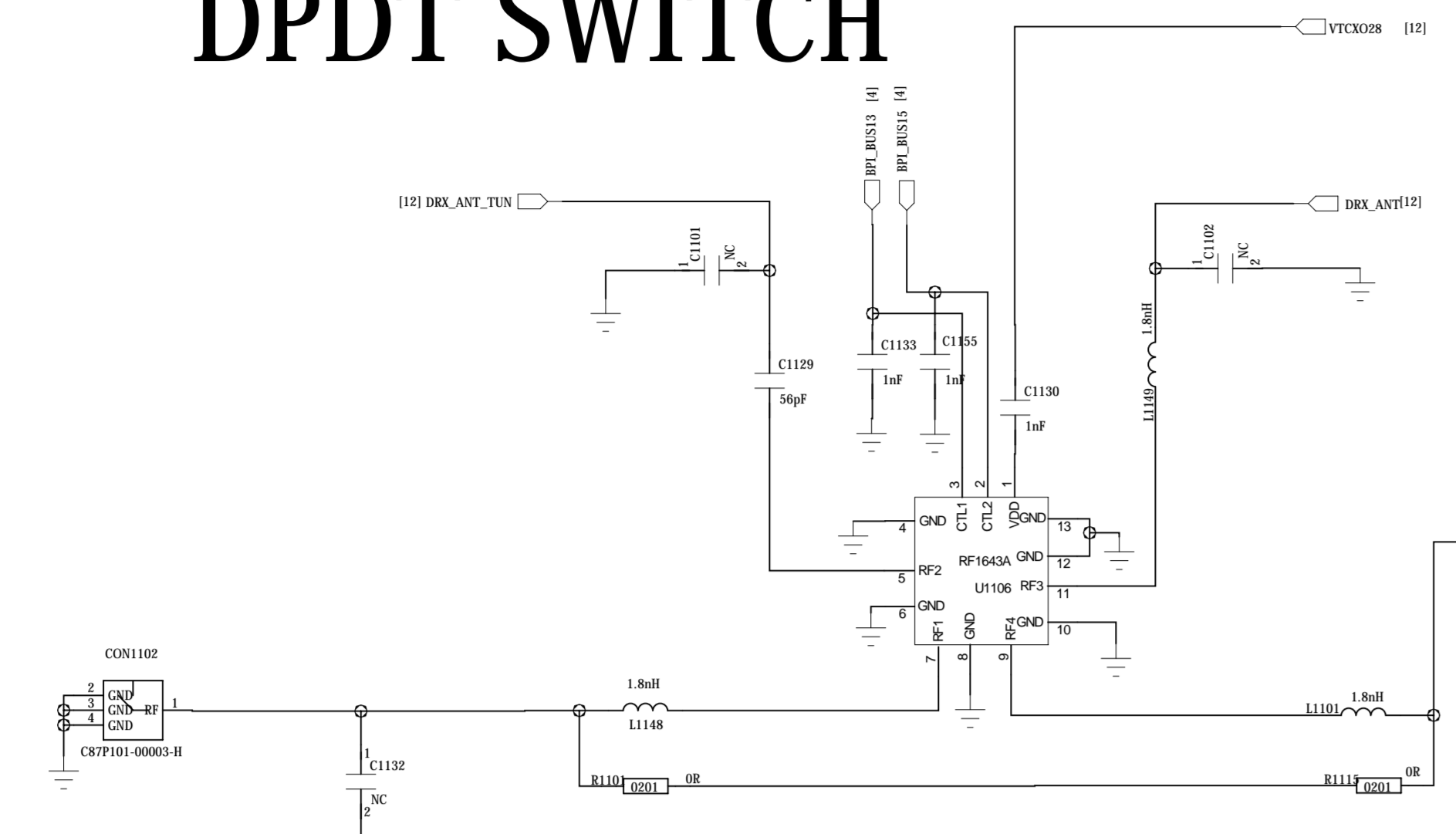
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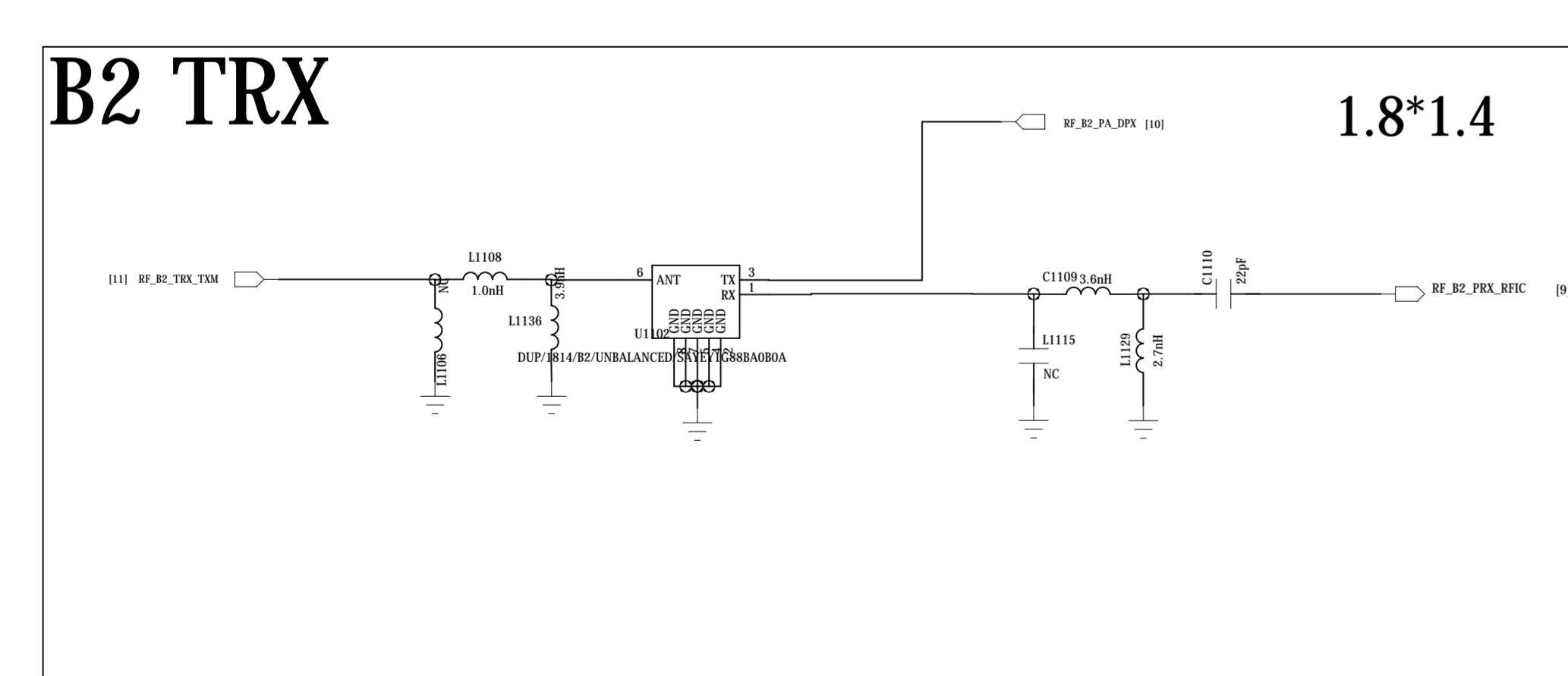
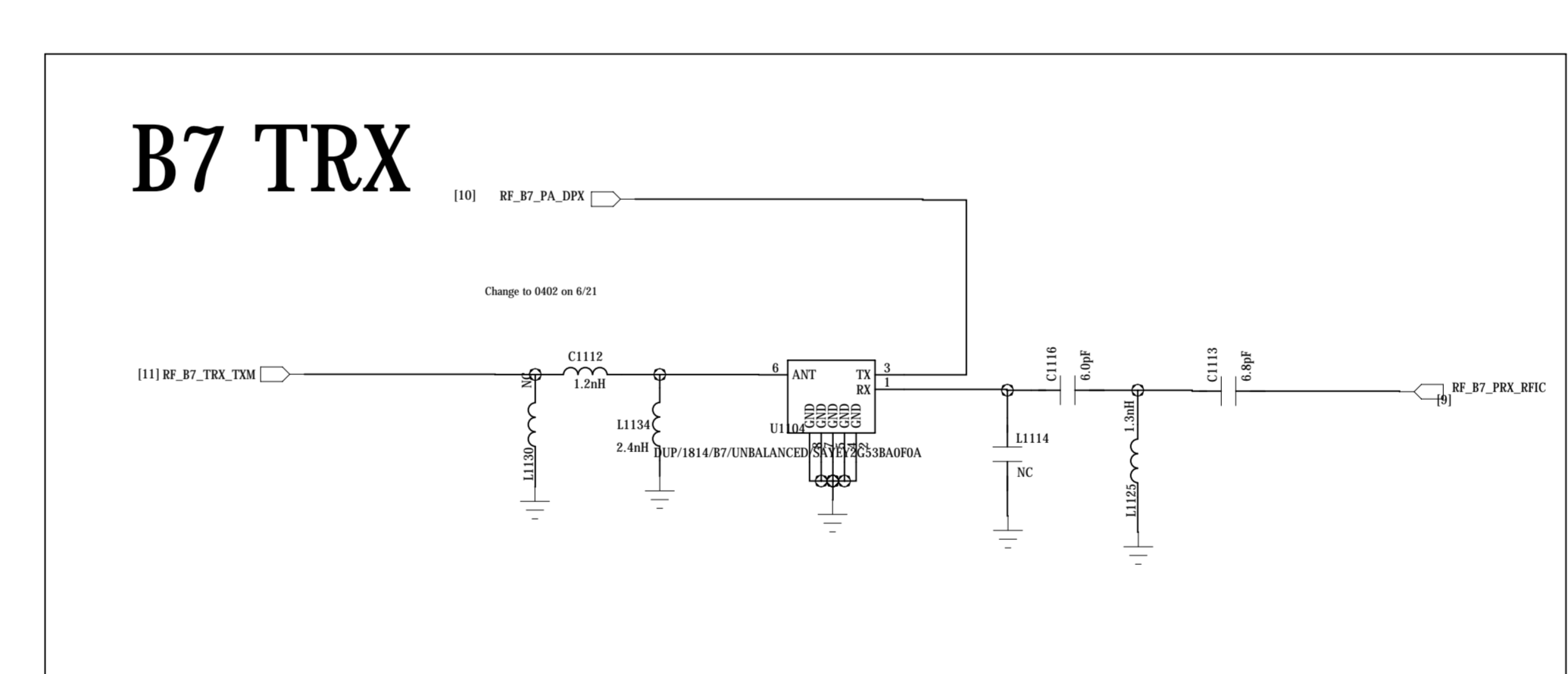
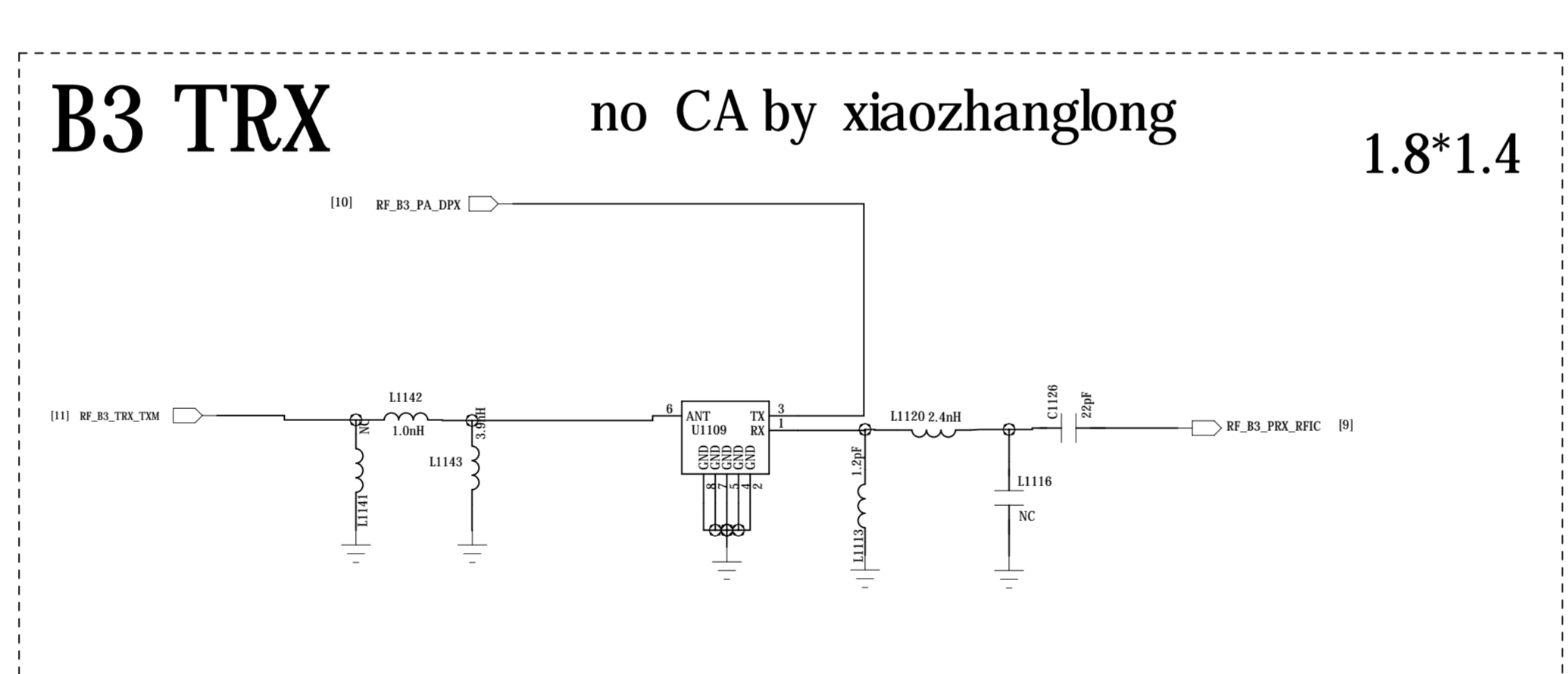
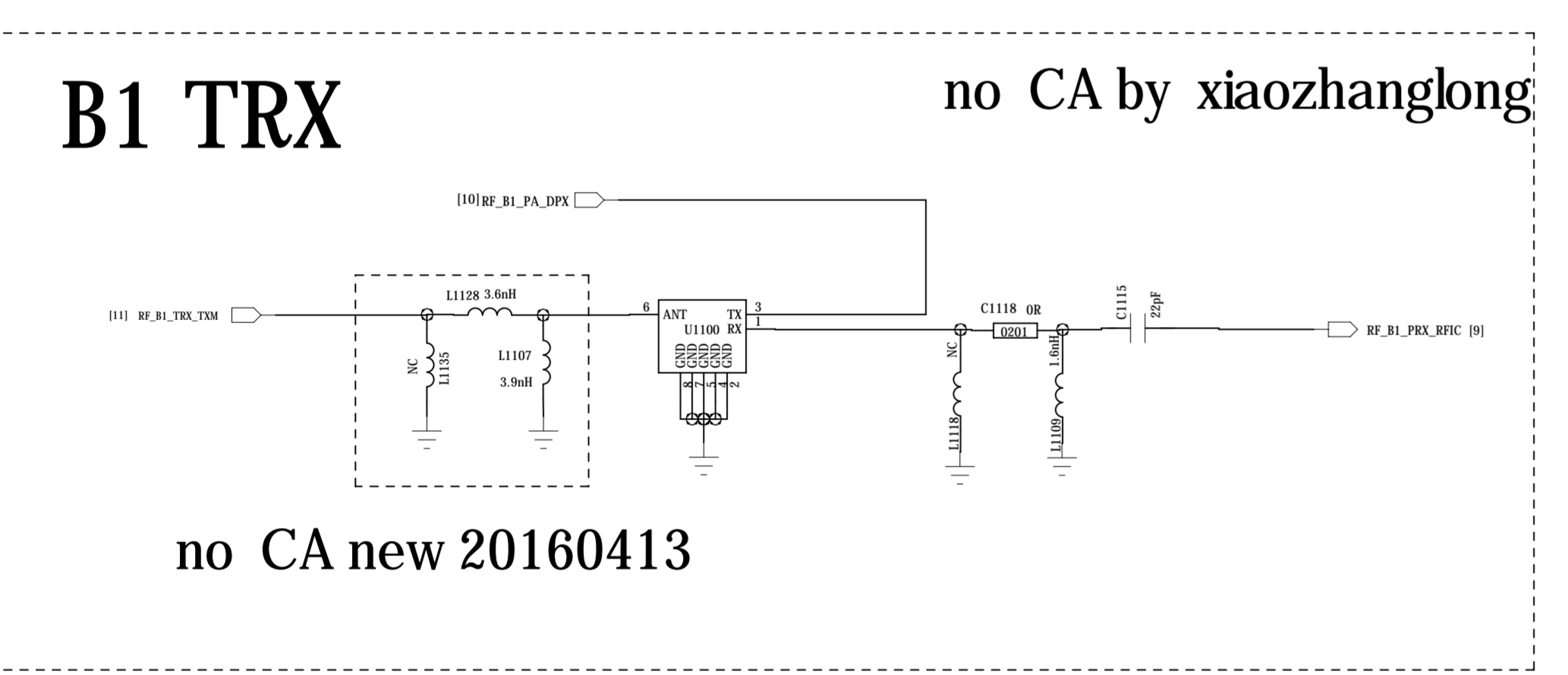
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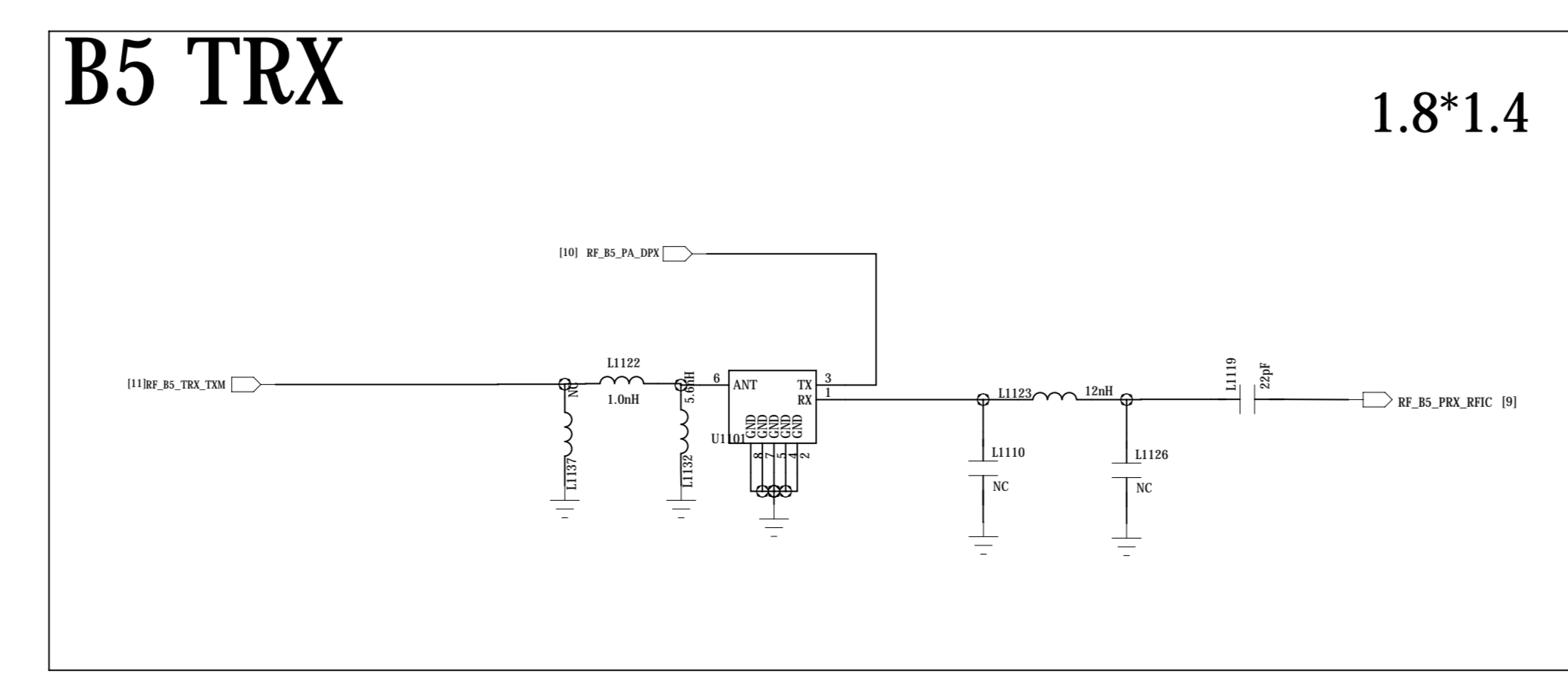
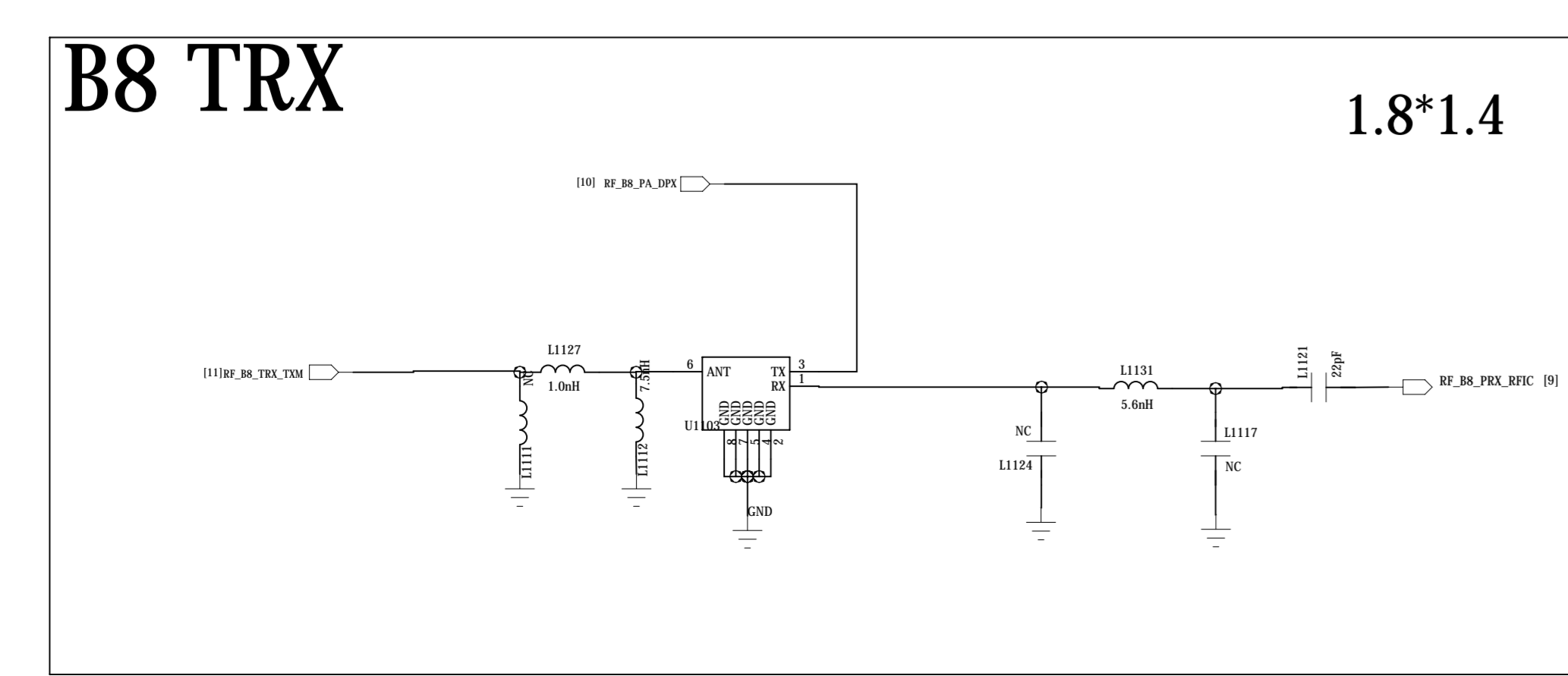
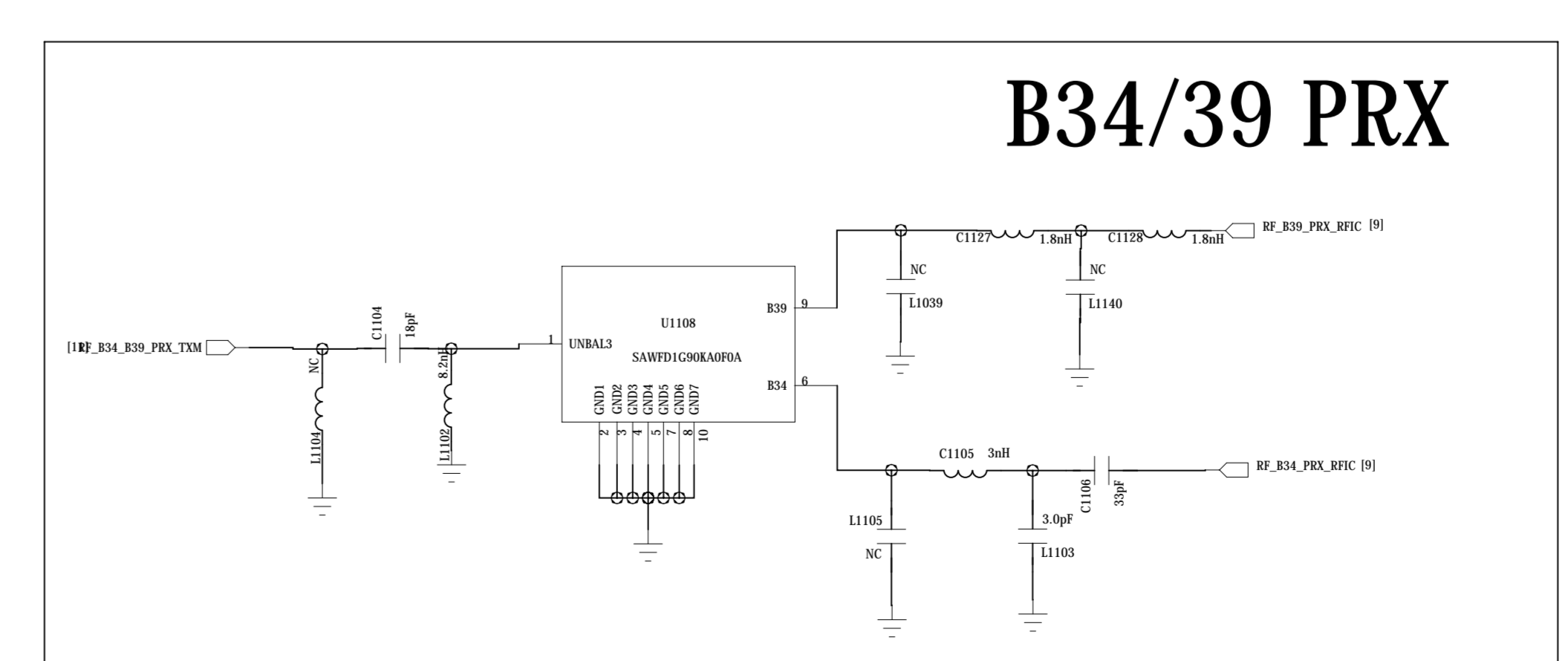
DPDT SWITCH



2G_PAIN_HB
2G_PAIN_LB



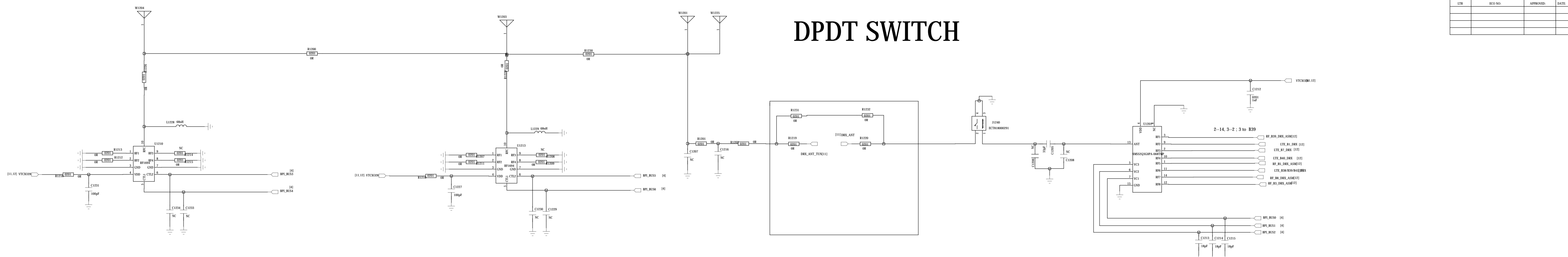
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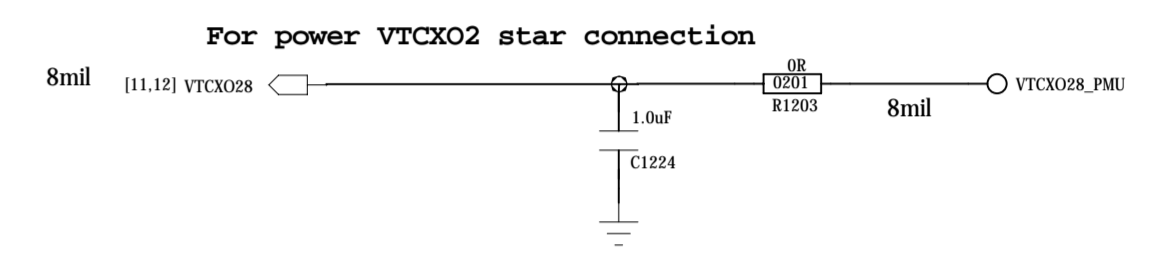
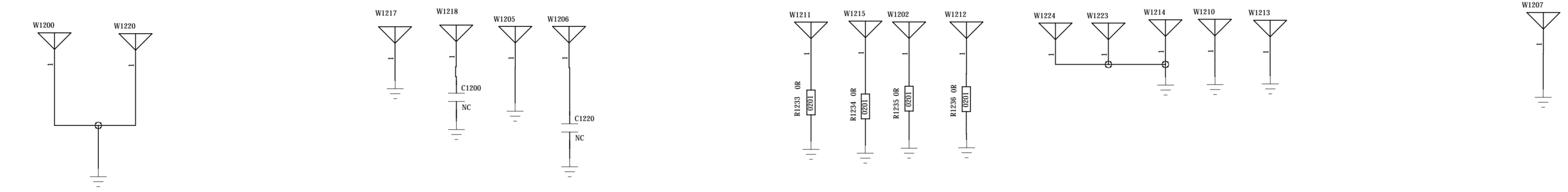
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DPDT SWITCH

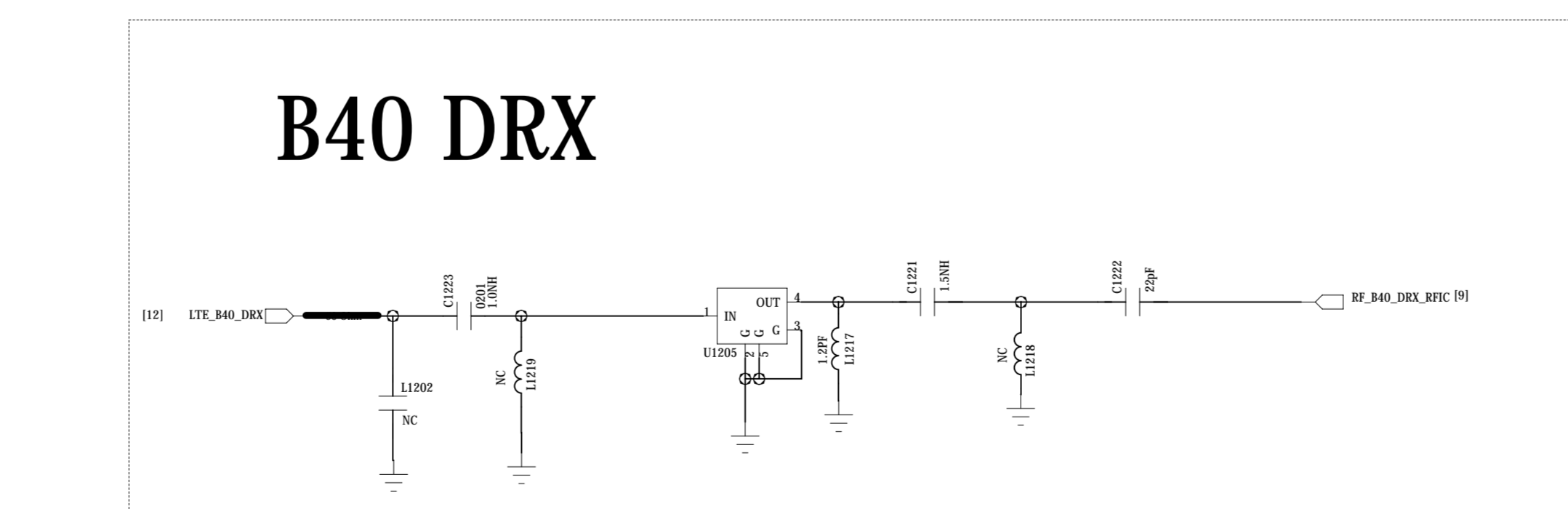
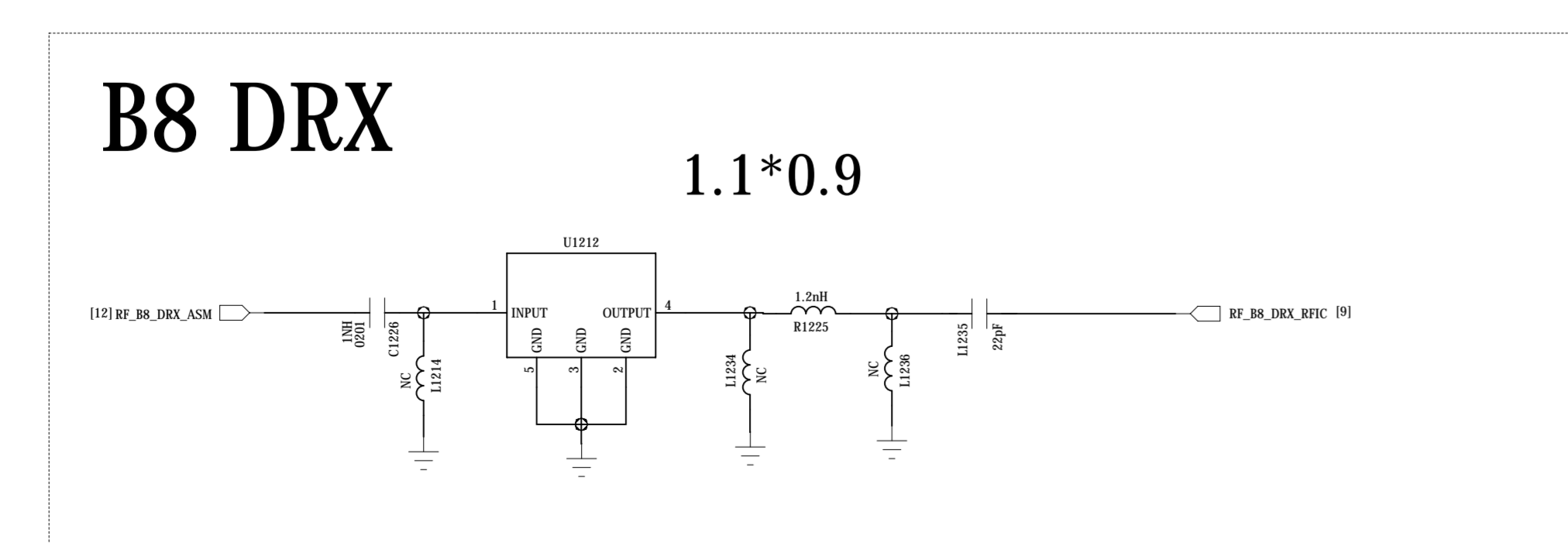
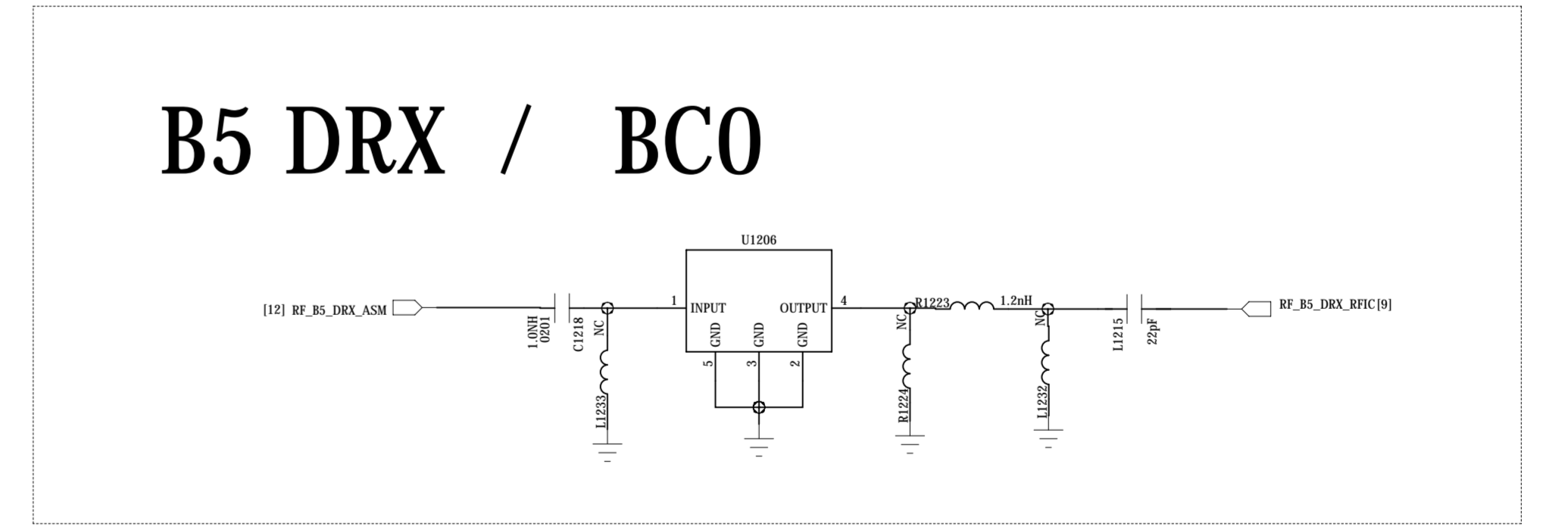
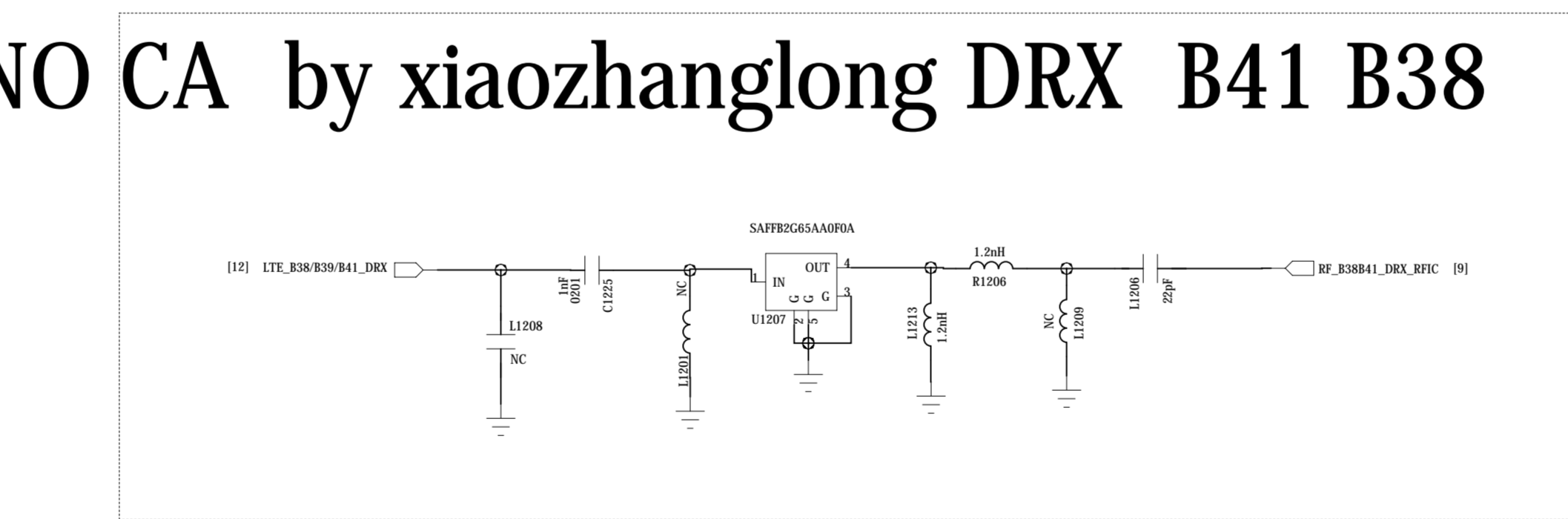
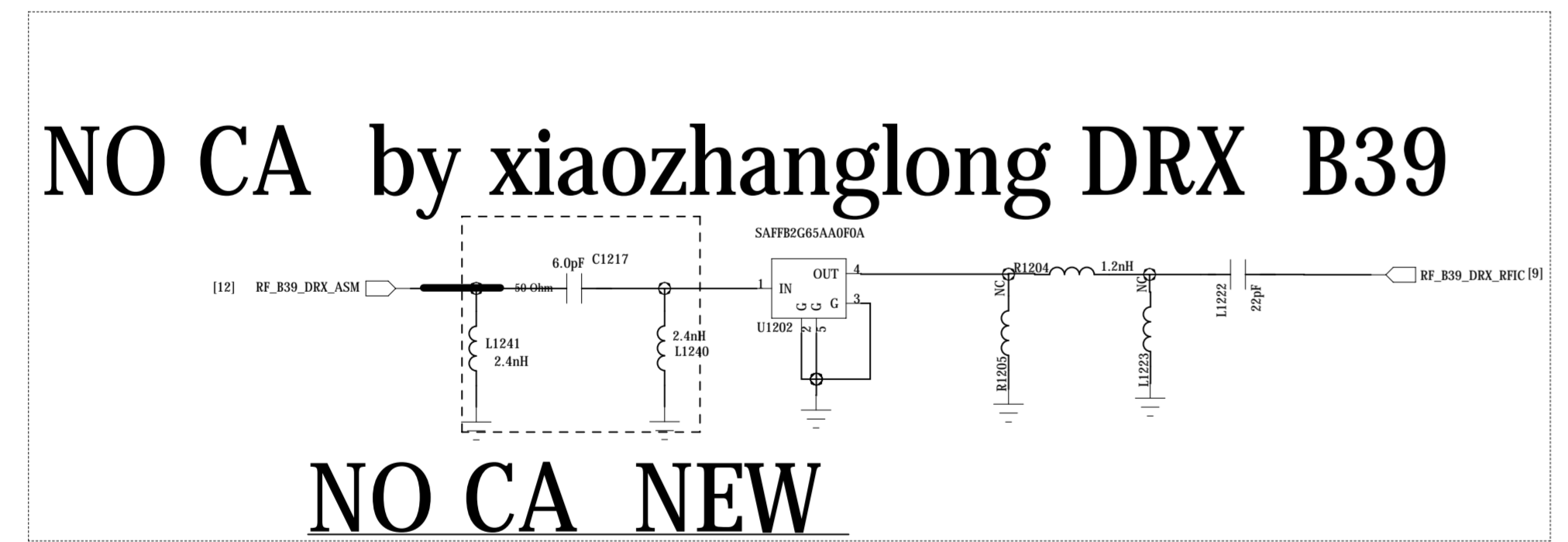
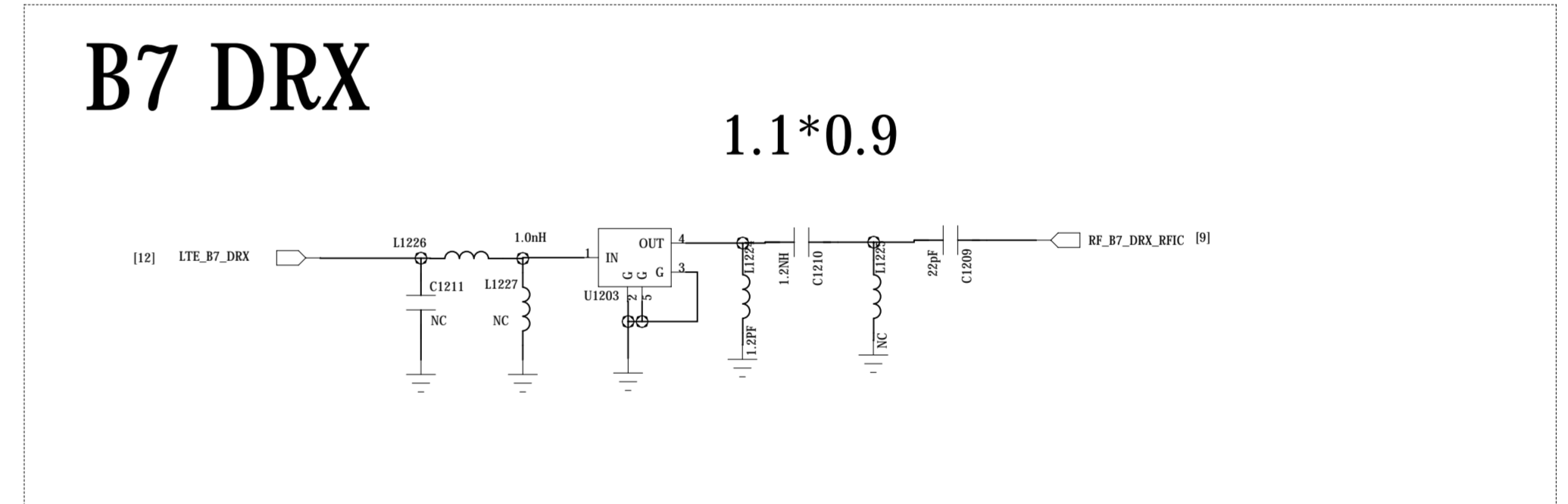
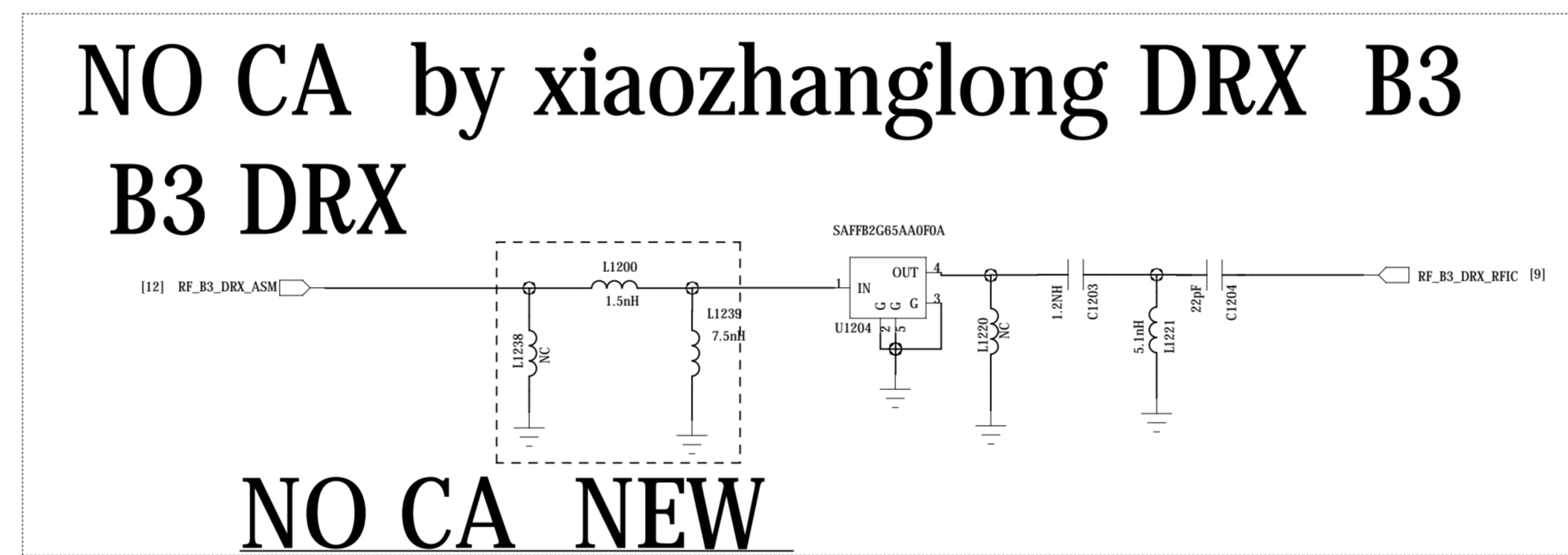
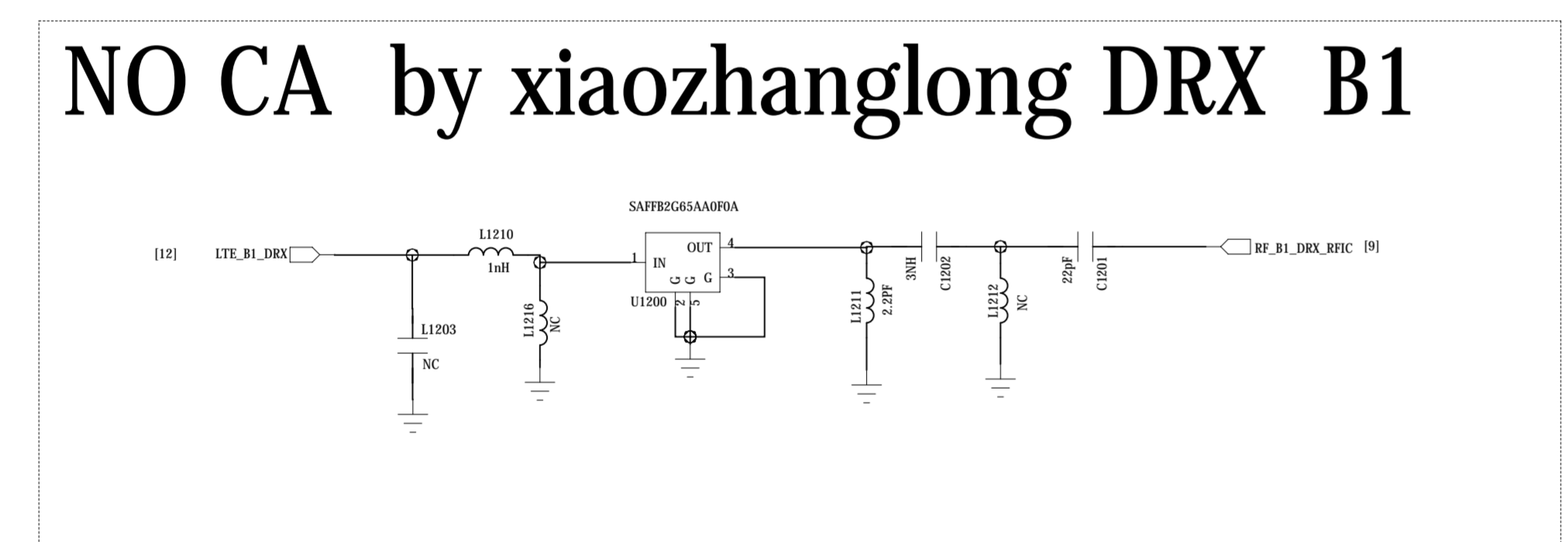


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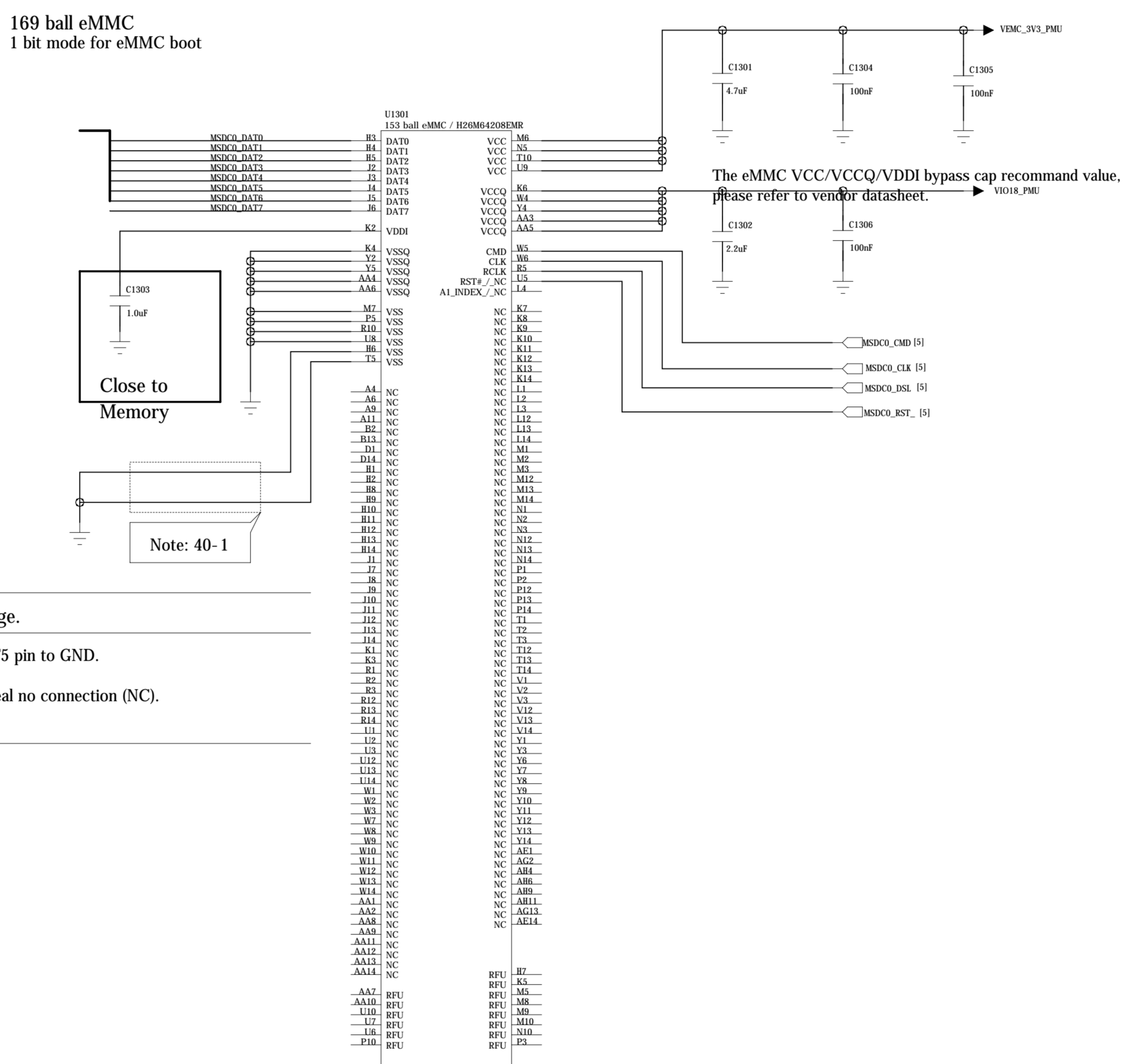


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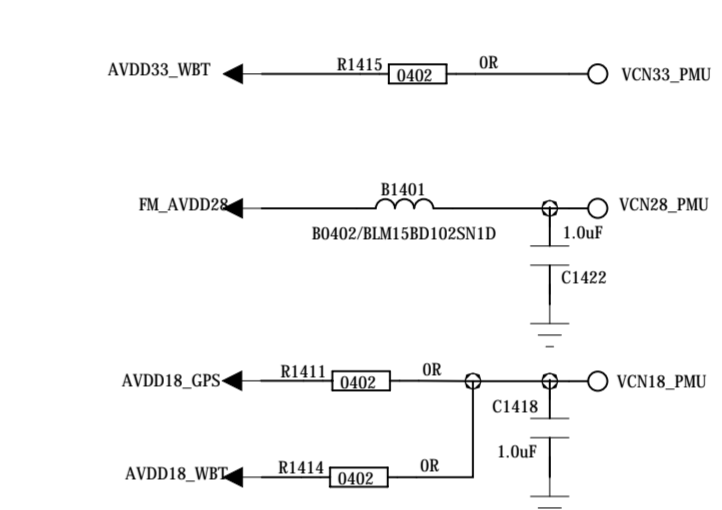
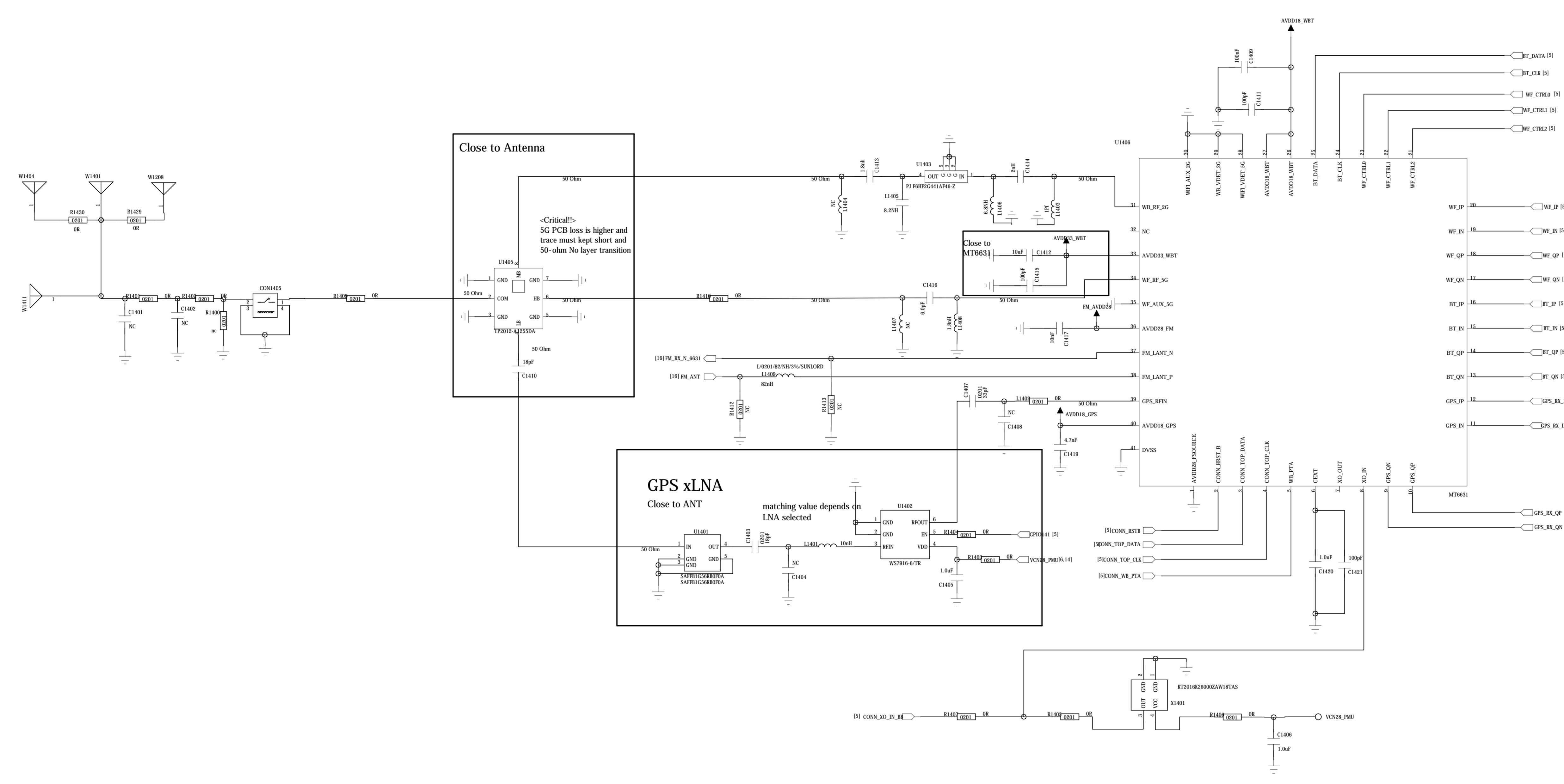
Schematic design notice of "40_MEMORY_eMMC" page.

Note 40-1: For eMMC 5.0/5.1, connect eMMC's H6 & T5 pin to GND.
 For eMMC 4.5, check eMMC's H6 & T5 is real no connection (NC).

DRAWN: <Drawn By>		DATED: <Drawn Date>		COMPANY: LC	
CHECKED: <Checked By>		DATED: <Checked Date>		TITLE: CX880	
QUALITY CONTROL: <QC By>		DATED: <QC Date>		CODE: <Code>	SIZE: A0
RELEASED: <Released By>		DATED: <Release Date>		DRAWING NO: <Drawing Number>	
		SCALE: <Scale>		REV: <Revision>	
				SHEET 48 20	

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ITS	ECO NO	APPROVED	DATE

Wifi & GPS & FM



Close to Antenna

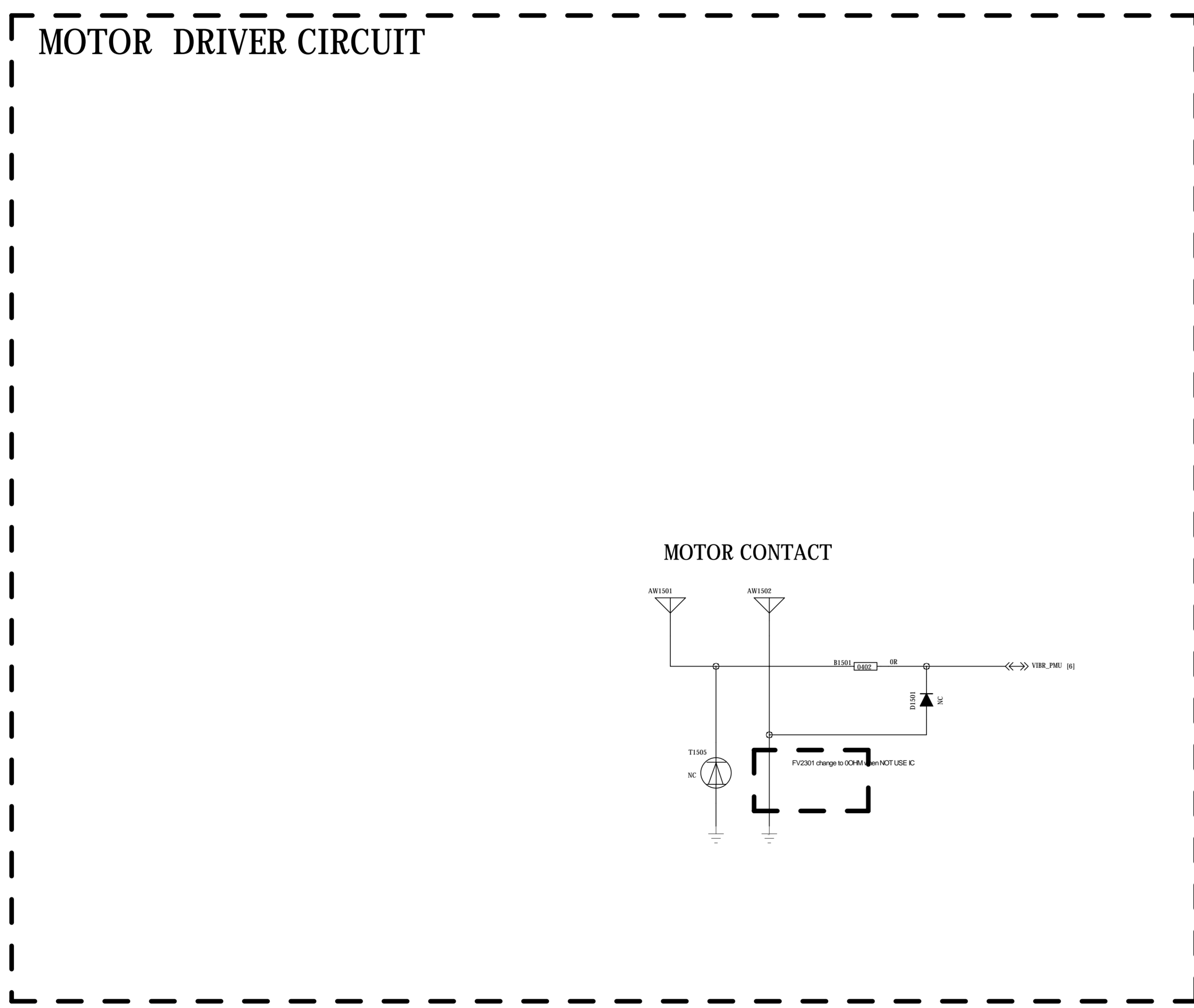
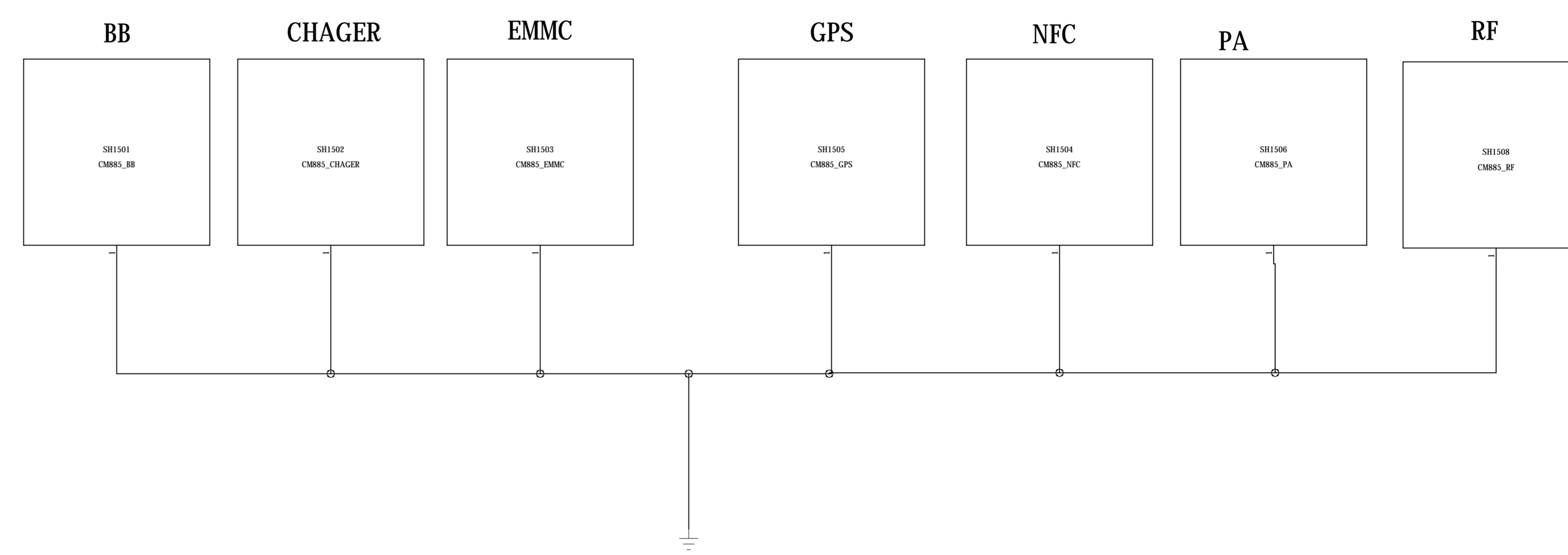
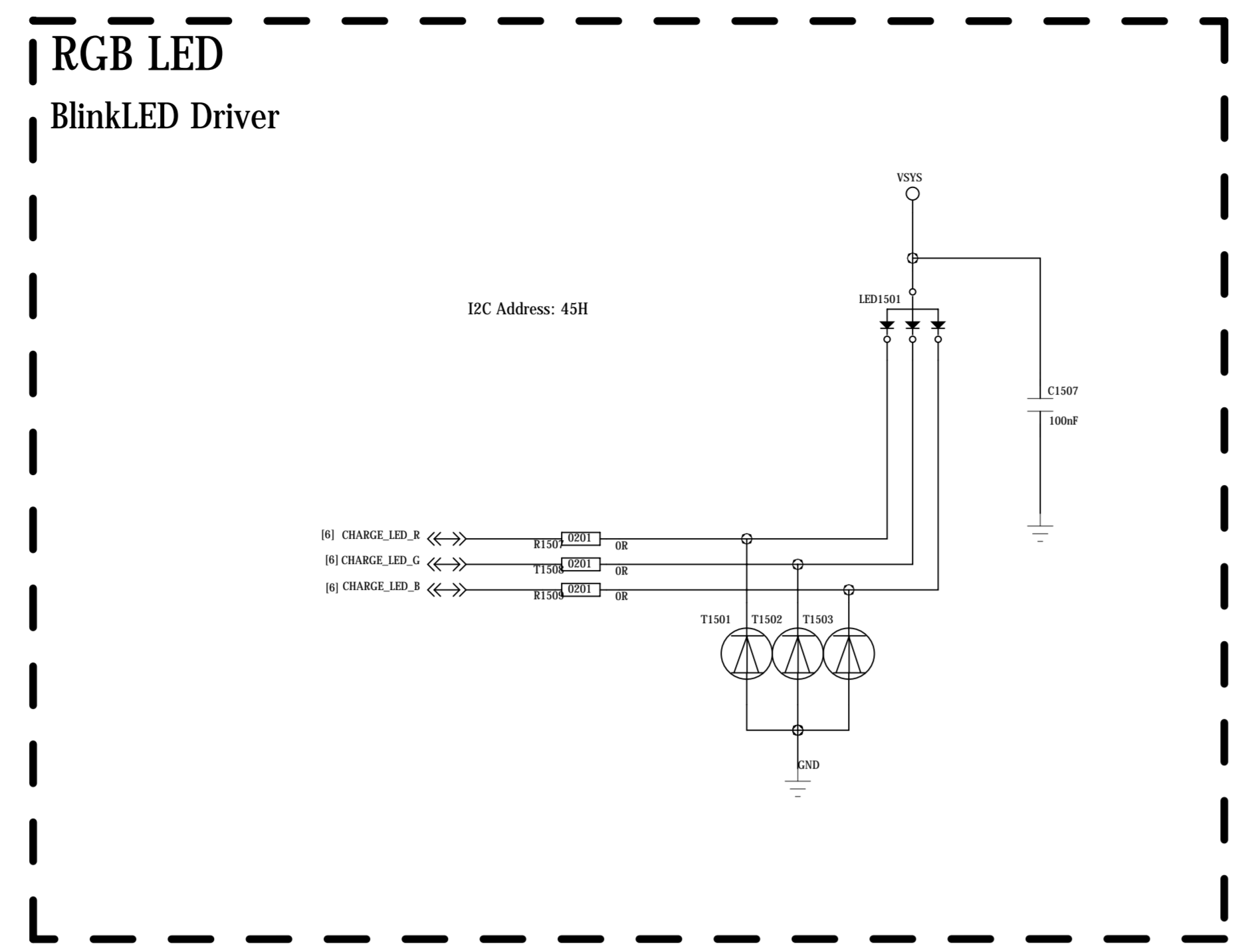
<Critical!>
5G PCB loss is higher and trace must kept short and 50-ohm. No layer transition

GPS xLNA
Close to ANT

matching value depends on LNA selected

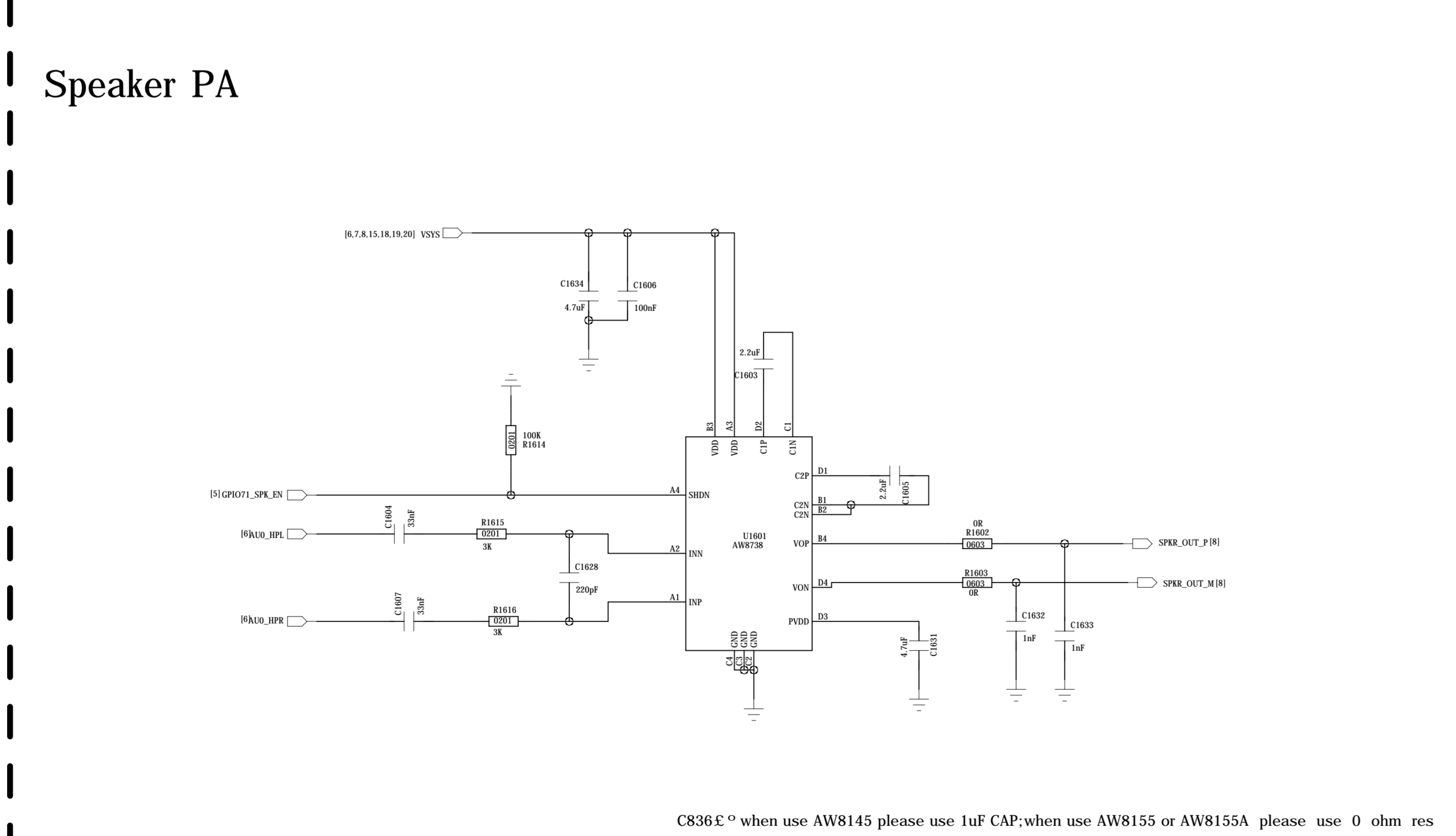
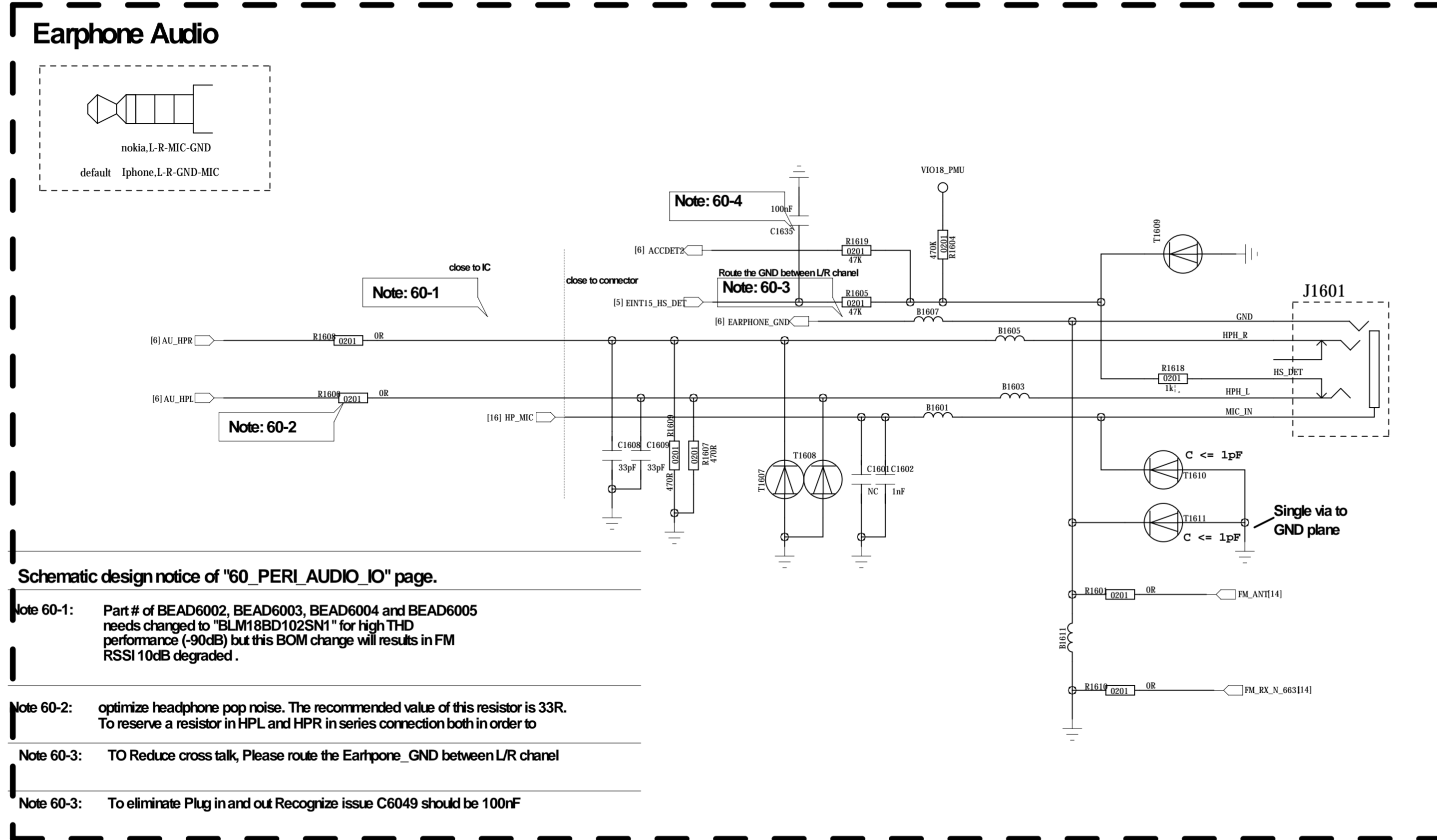
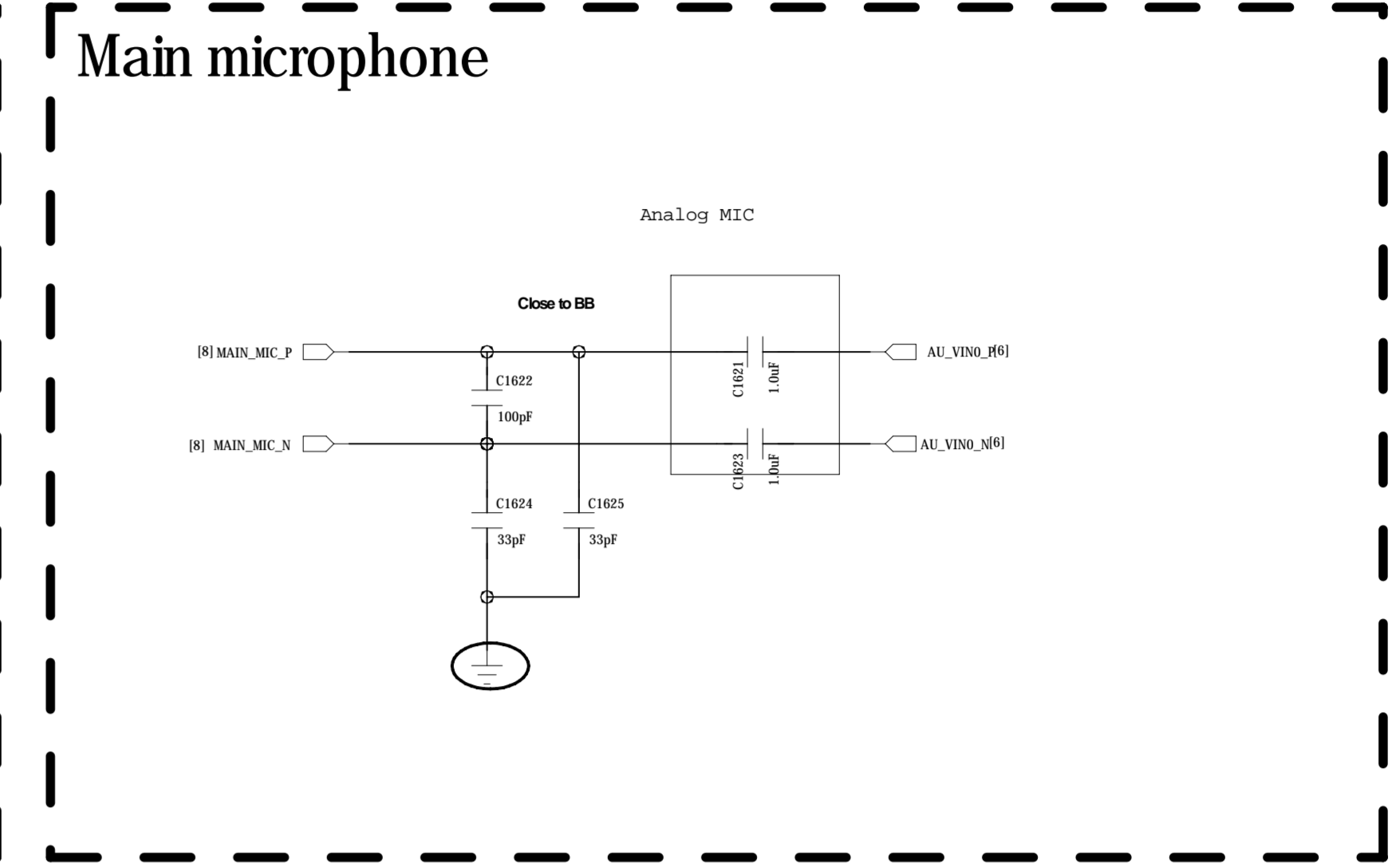
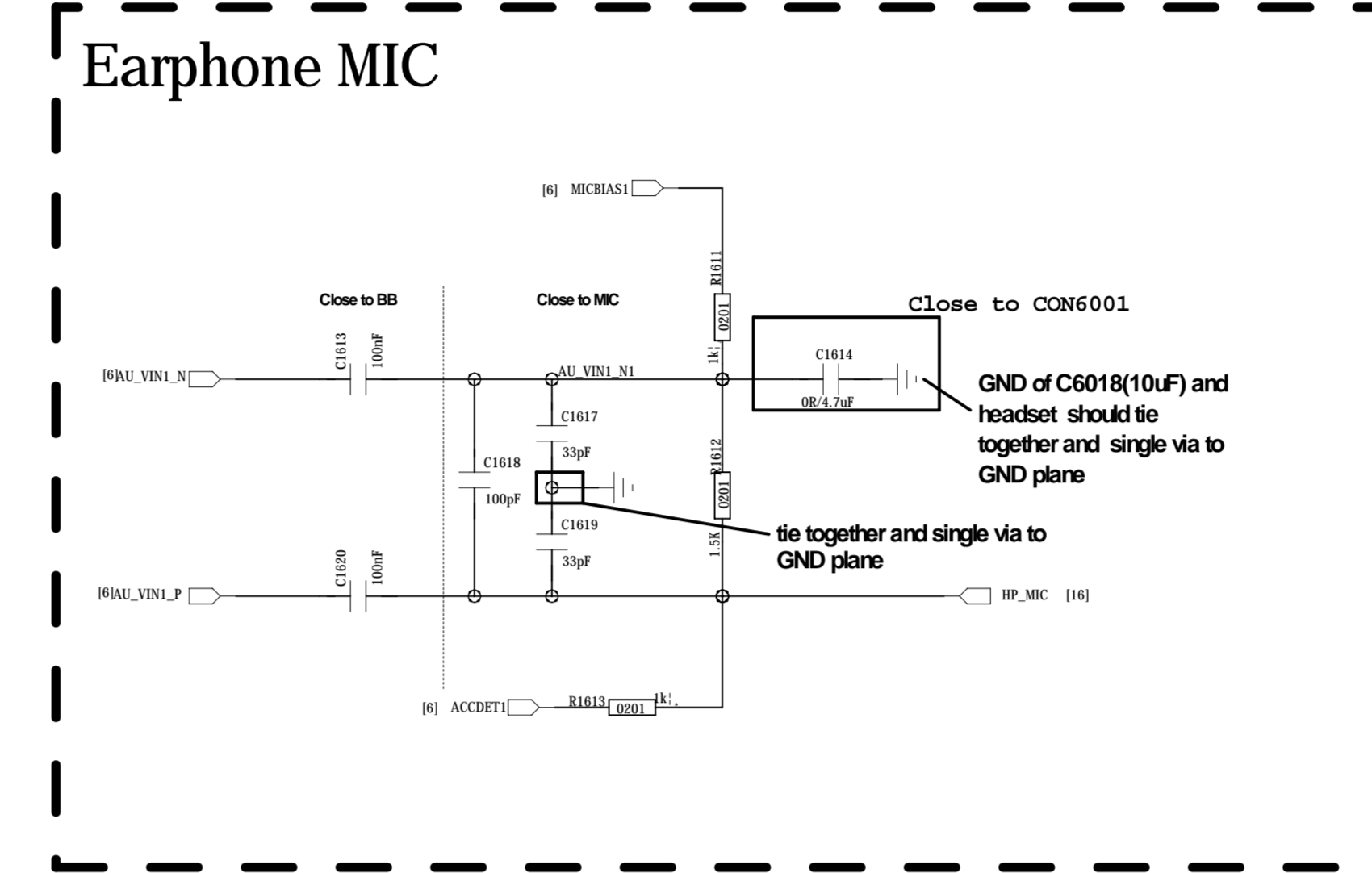
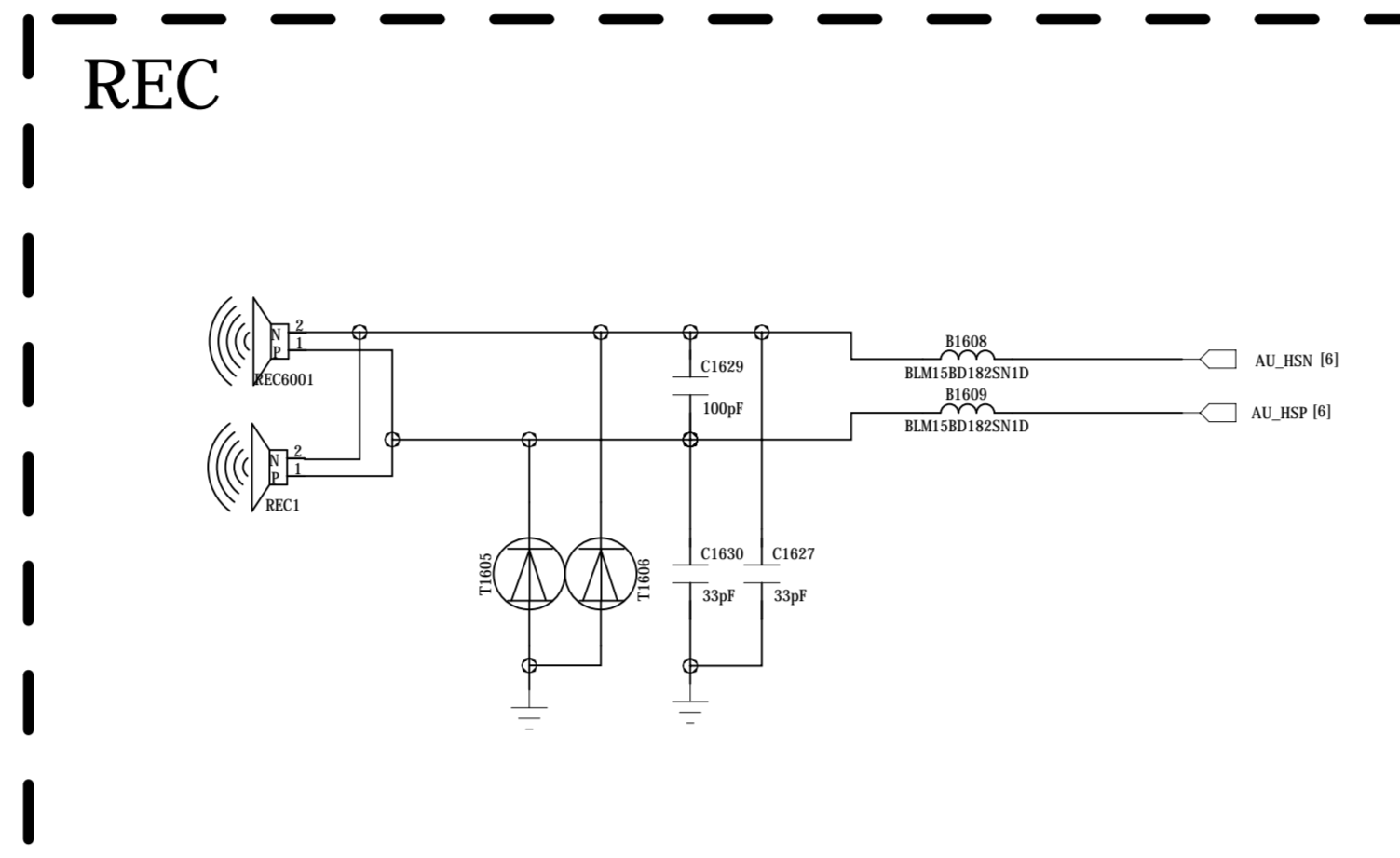
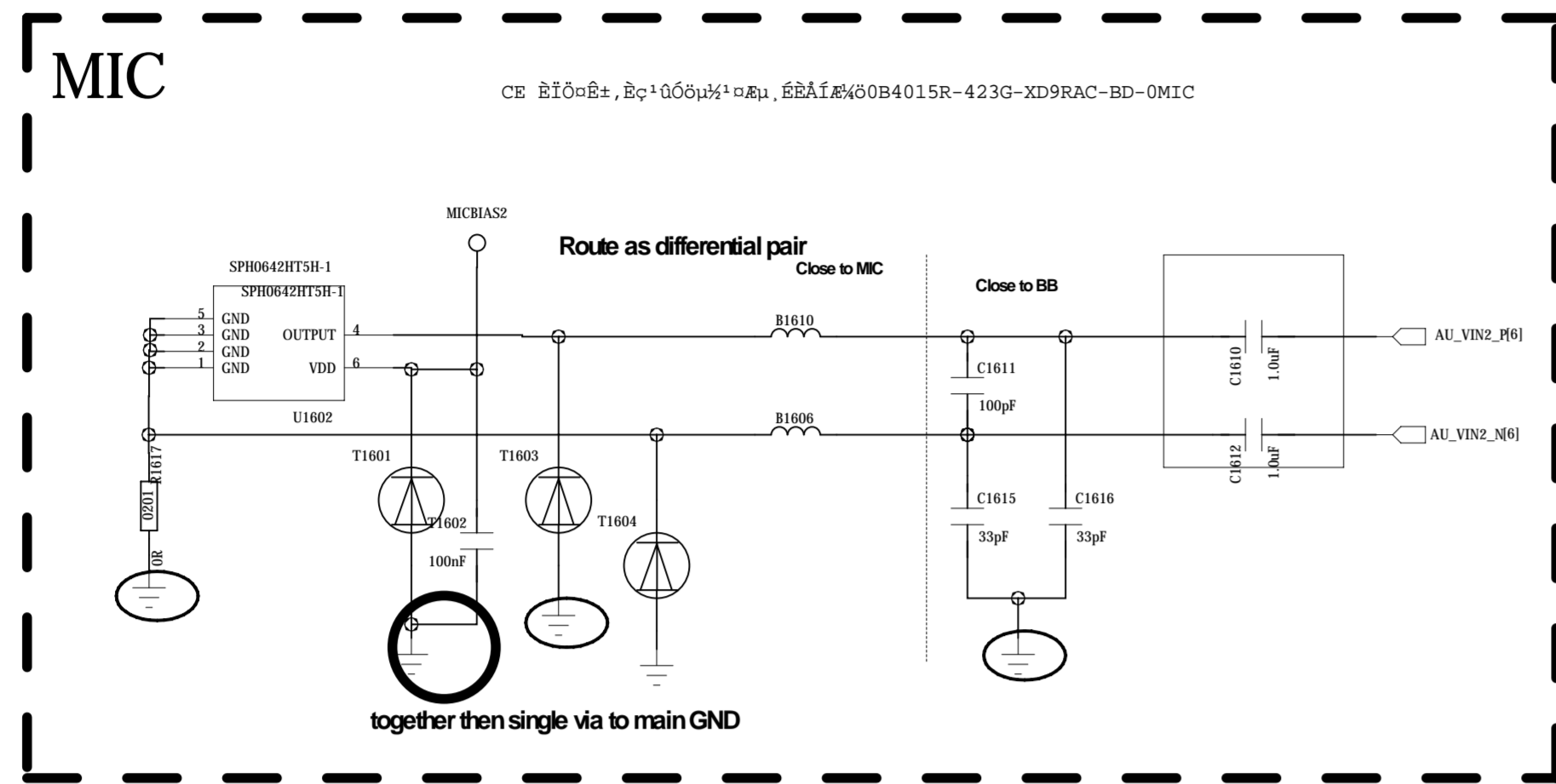
COMPANY:		LC	
TITLE:		CX880	
DRAWN:	<Drawn By>	DATE:	<Drawn Date>
CHECKED:	<Checked By>	DATE:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATE:	<QC Date>
RELEASED:	<Released By>	DATE:	<Release Date>
CORR:	SIZE:	DRAWING NO:	REV:
<Code>		A0 <Drawing Number> Revision	
SCALE:	<Scale>	SHEET:	14 20

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REV	REV NO.	APPROVED	DATE



DRAWN: <Drawn By>		DATE: <Drawn Date>		COMPANY: LC	
CHECKED: <Checked By>		DATE: <Checked Date>		TITLE: CX880	
QUALITY CONTROL: <QC By>		DATE: <QC Date>		CODE: <Code>	SIZE: A0
RELEASED: <Released By>		DATE: <Release Date>		DRAWING NO: <Drawing Number> REVISION: <Revision>	
SCALE: <Scale>				SHEET 46 20	

REVISION RECORD			
ITR	ECO NO	APPROVED	DATE



Schematic design notice of "60_PERI_AUDIO_IO" page.

Note 60-1: Part # of BEAD6002, BEAD6003, BEAD6004 and BEAD6005 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will result in FM RSSI 10dB degraded.

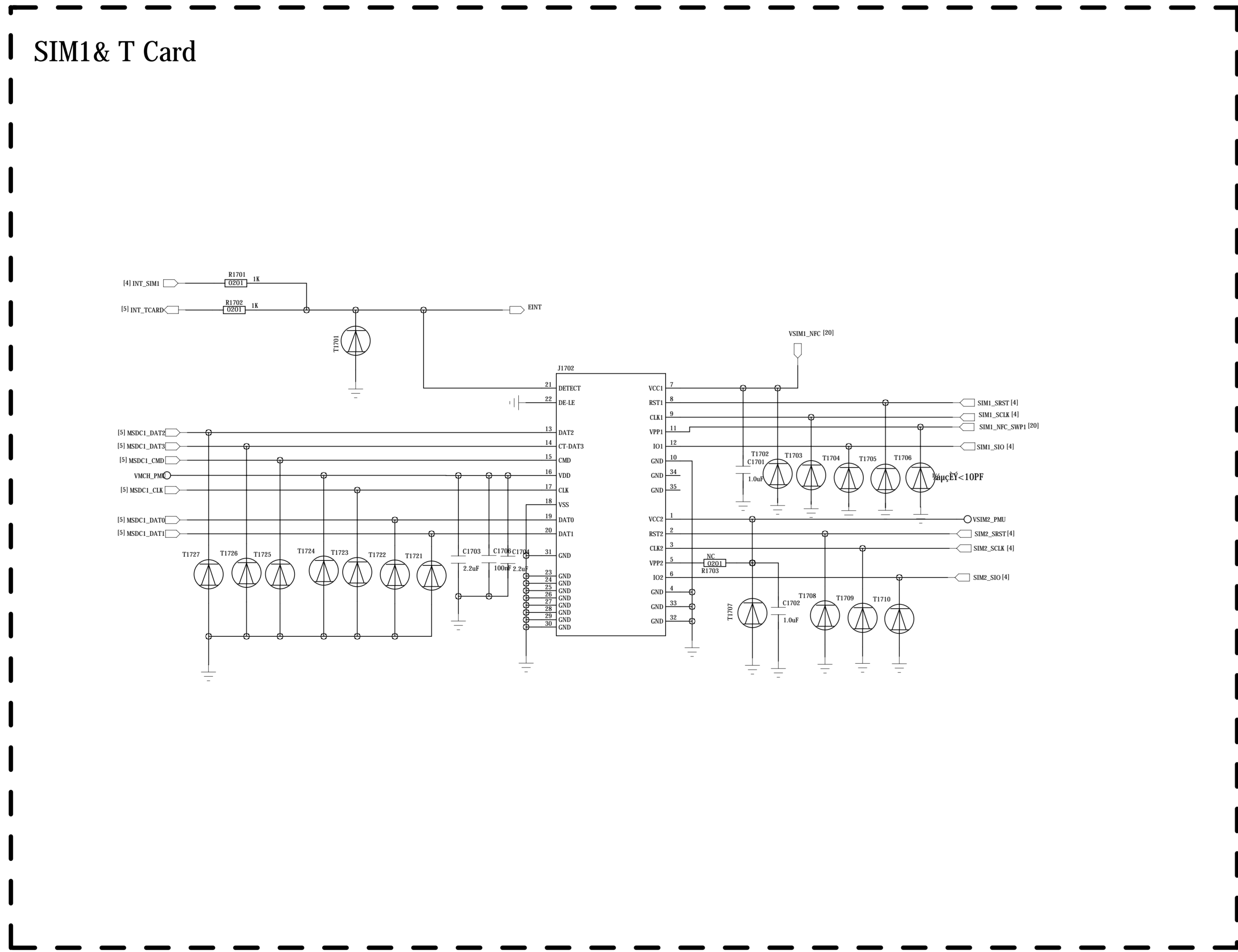
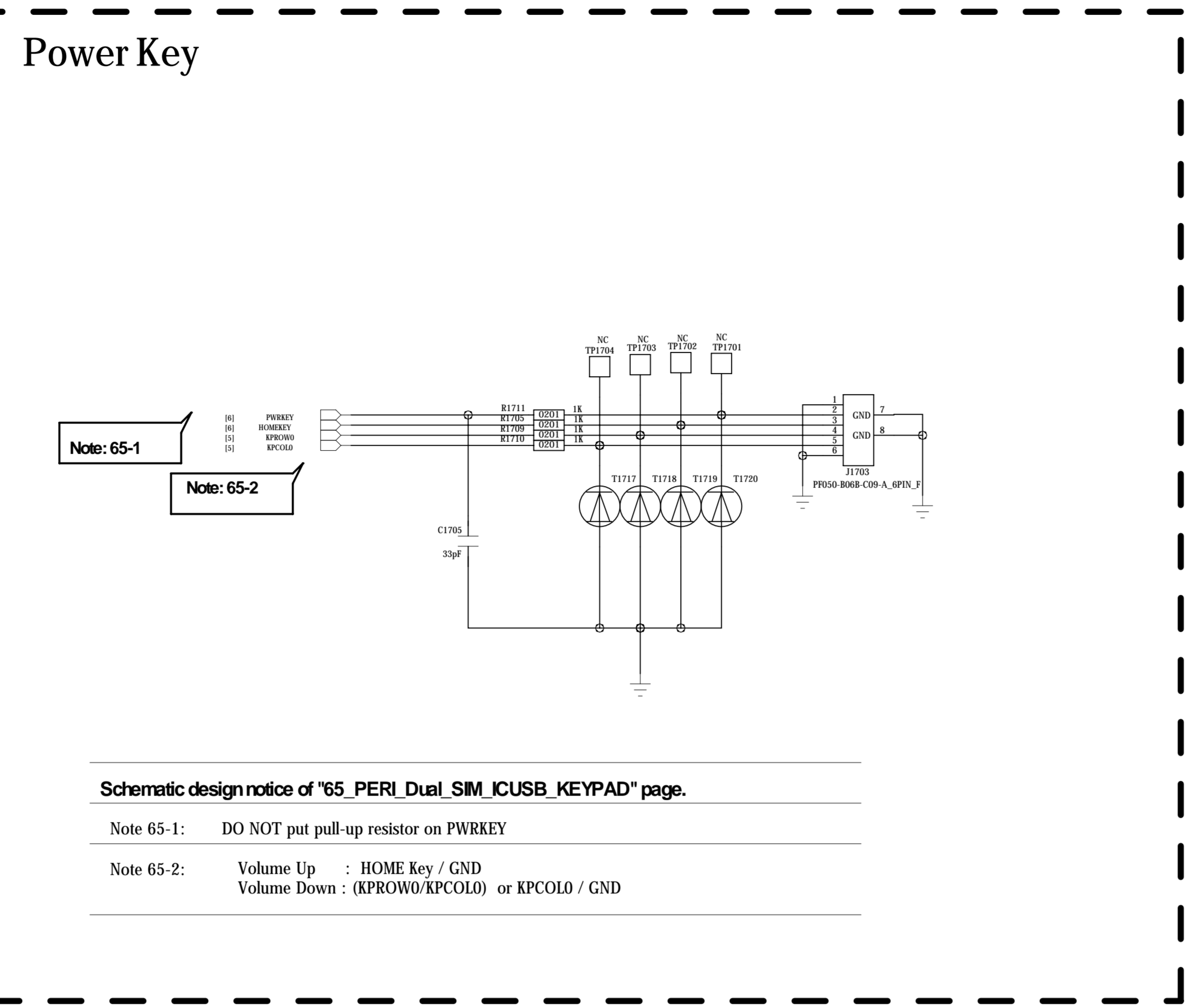
Note 60-2: optimize headphone pop noise. The recommended value of this resistor is 33R. To reserve a resistor in HPL and HPR in series connection both in order to

Note 60-3: TO Reduce cross talk, Please route the Earphone_GND between L/R channel

Note 60-3: To eliminate Plug in and out Recognize issue C6049 should be 100nF

COMPANY:		LC	
TITLE:		CX880	
DRAWN:	<Drawn By>	DATE:	<Drawn Date>
CHECKED:	<Checked By>	DATE:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATE:	<QC Date>
RELEASED:	<Released By>	DATE:	<Release Date>
CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A0	<Drawing Number>	<Revision>
SCALE:	<Scale>	SHEET:	46 20

REVISION RECORD			
LT#	REV NO.	APPROVED	DATE

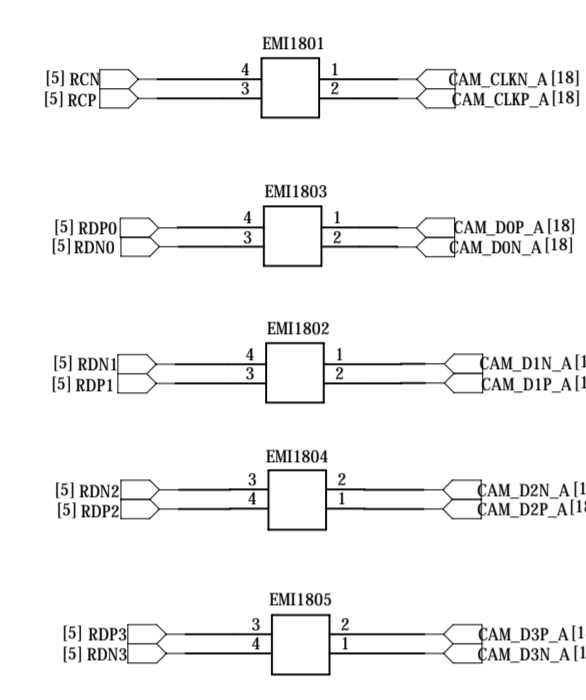
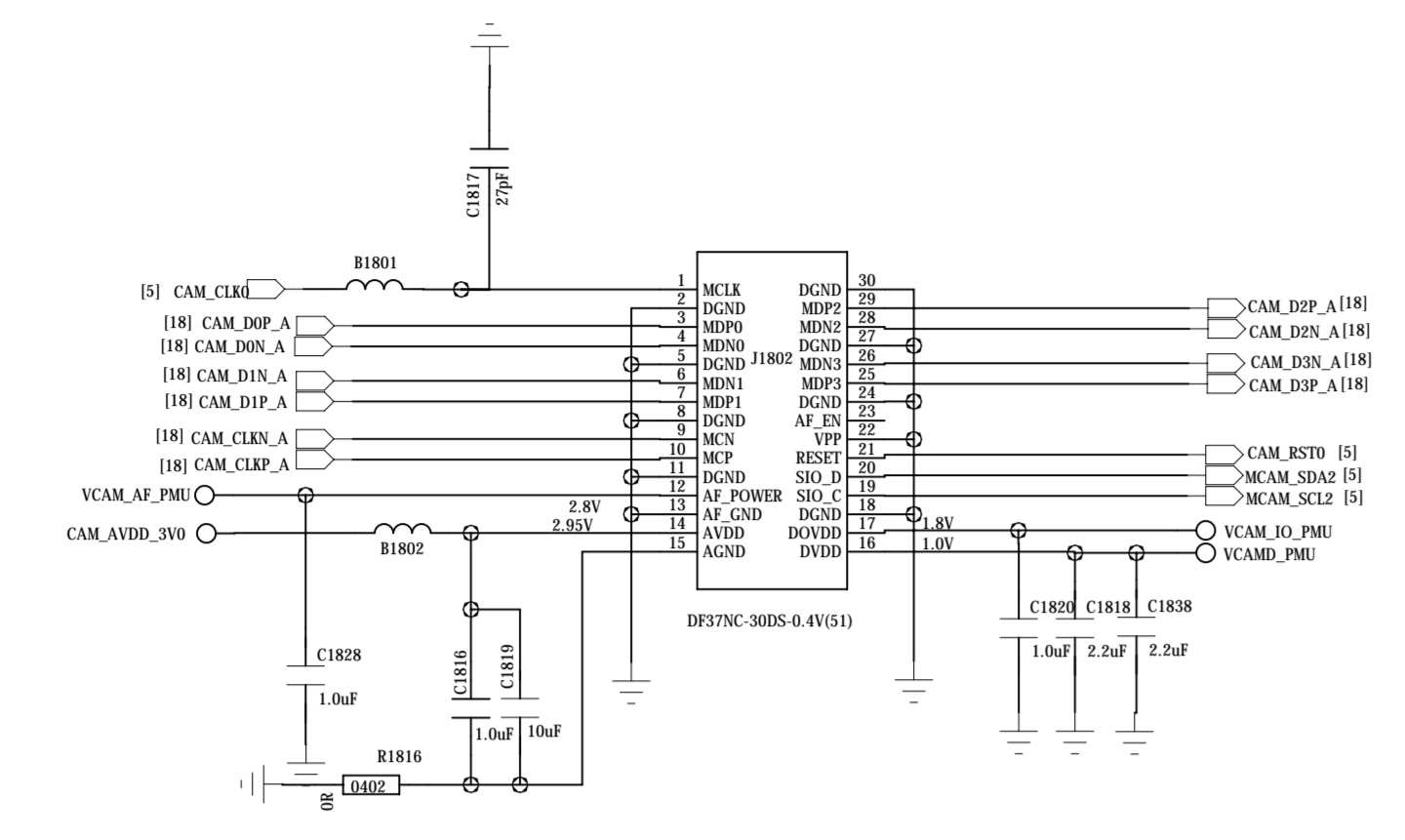


DRAWN: <Drawn By>		DATED: <Drawn Date>		COMPANY: LC	
CHECKED: <Checked By>		DATED: <Checked Date>		TITLE: CX880	
QUALITY CONTROL: <QC By>		DATED: <QC Date>		CODE: <Code>	SIZE: A0
RELEASED: <Released By>		DATED: <Release Date>		DRAWING NO: <Drawing Number> Revision: <Revision>	
SCALE: <Scale>		SHEET: 17		20	

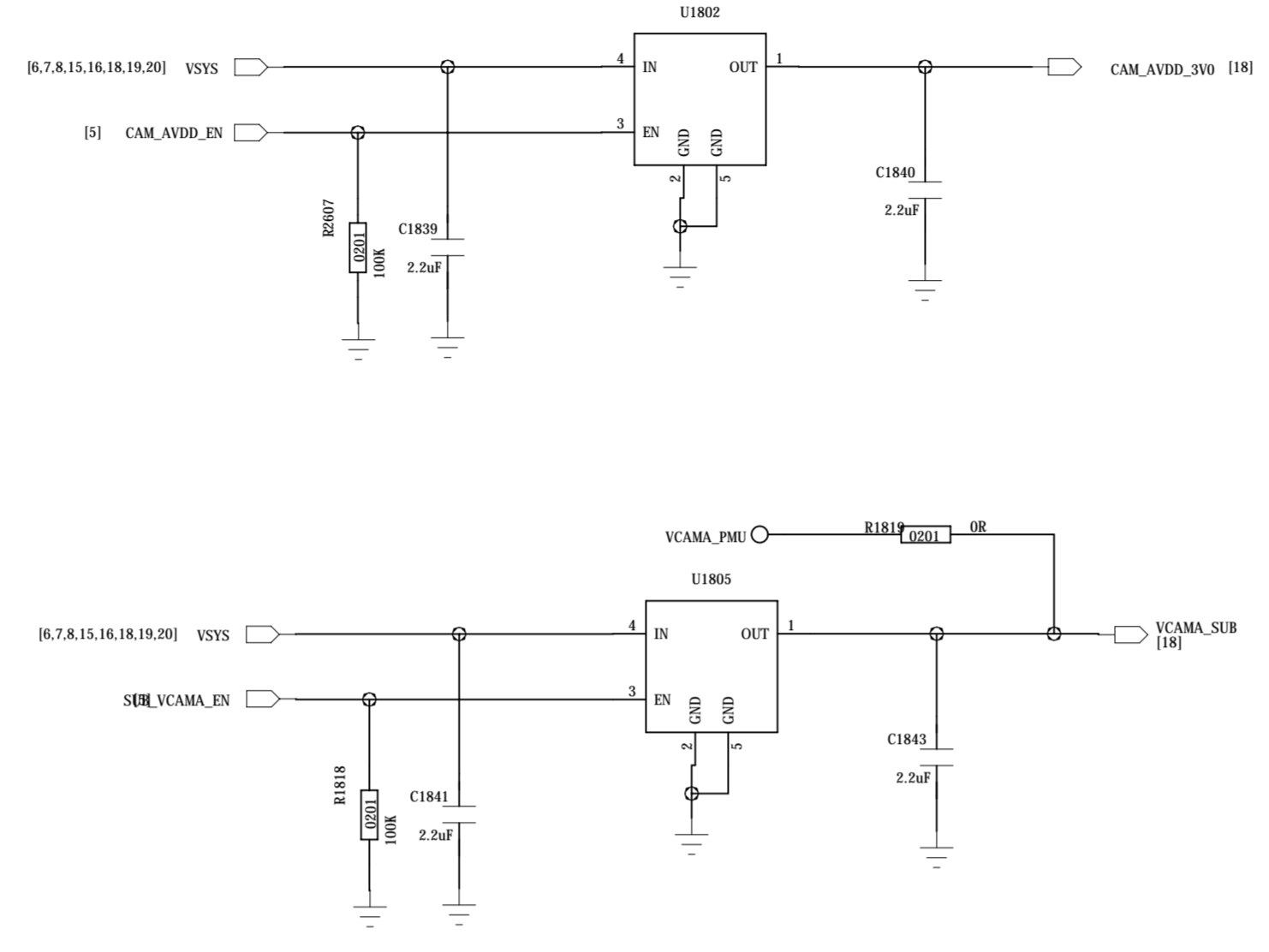
REVISION RECORD			
LT#	ECO NO.	APPROVED	DATE

Main Camera A

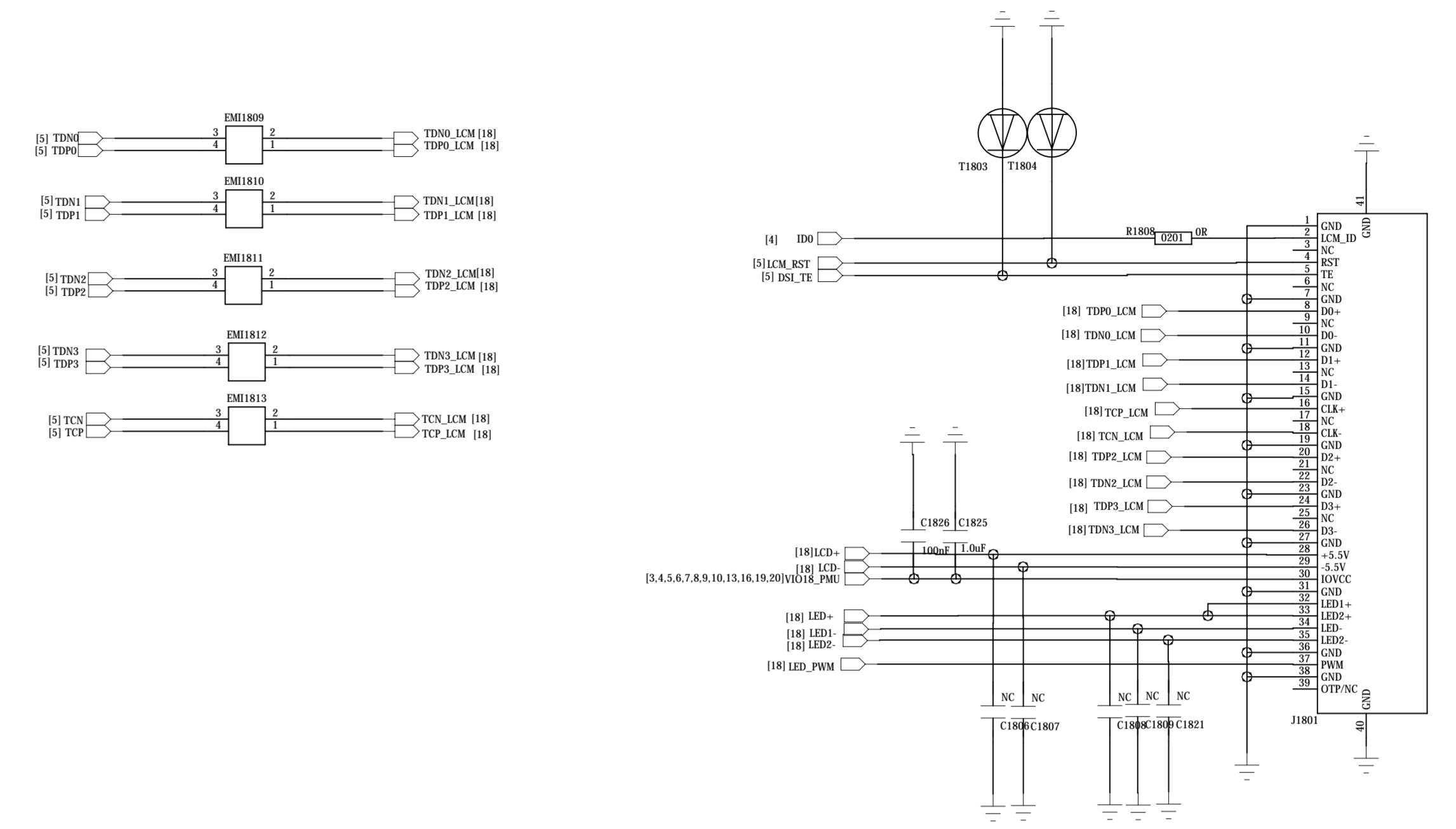
Main Camera



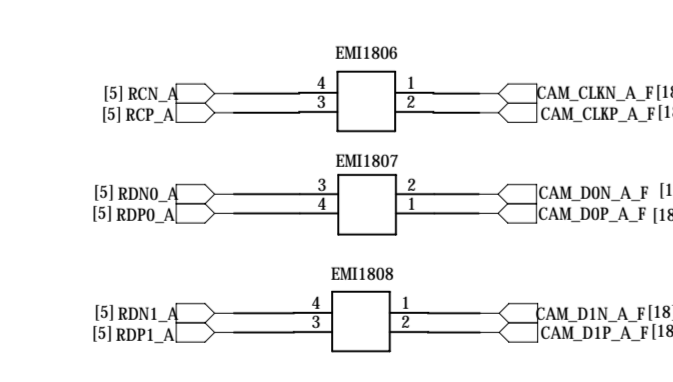
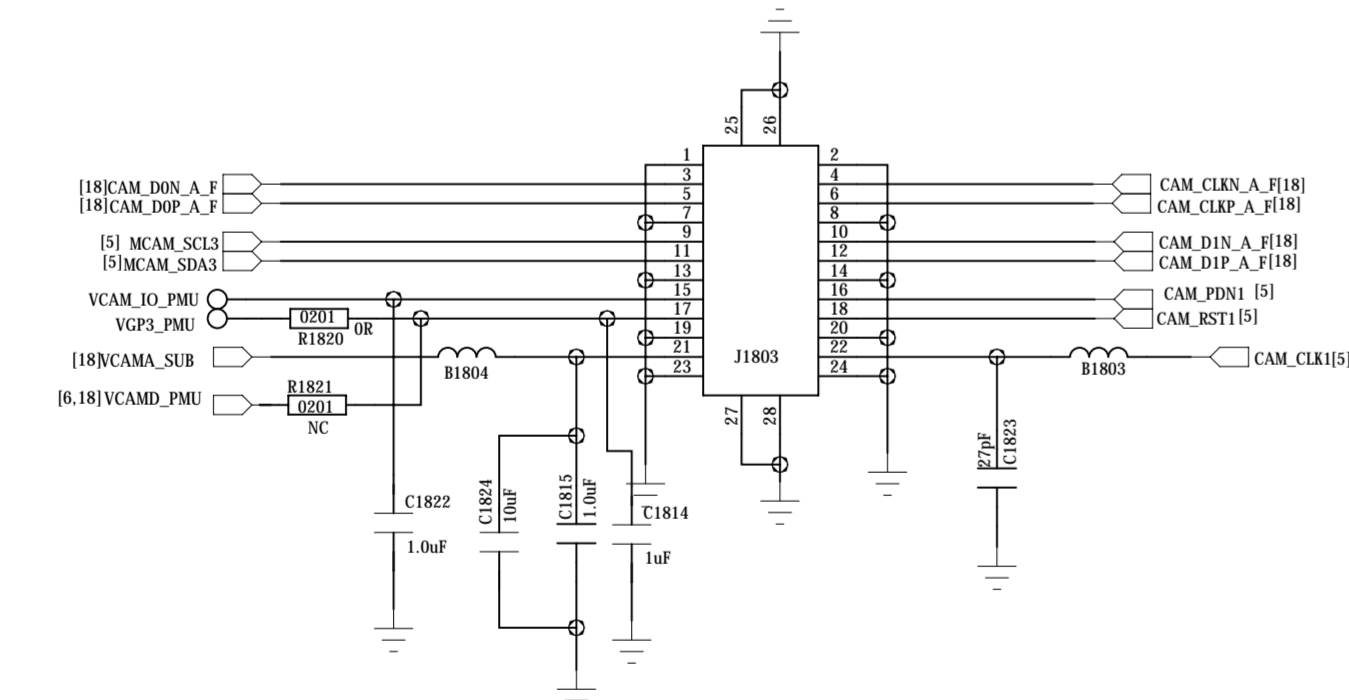
Main Camera AVDD



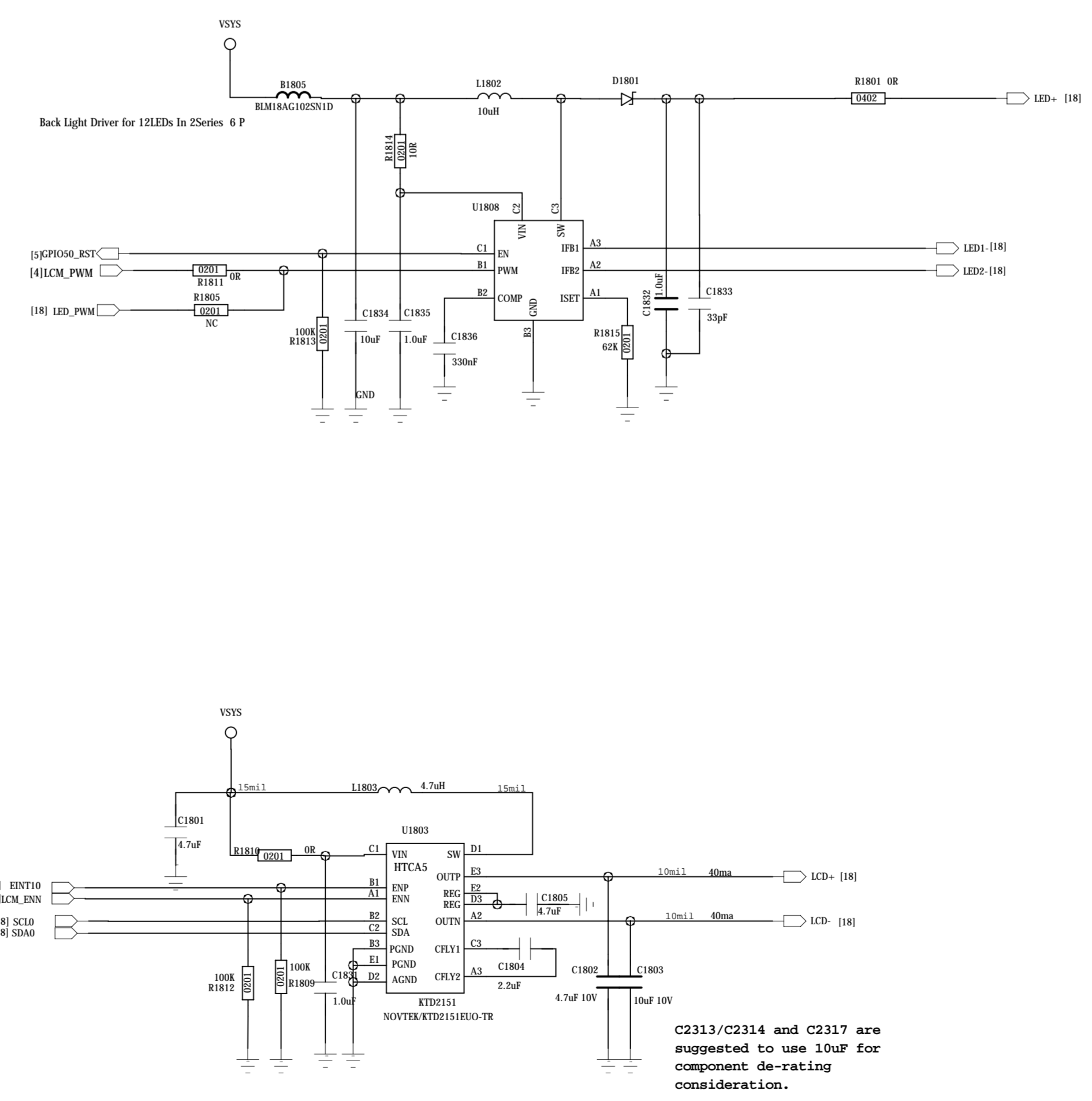
LCM



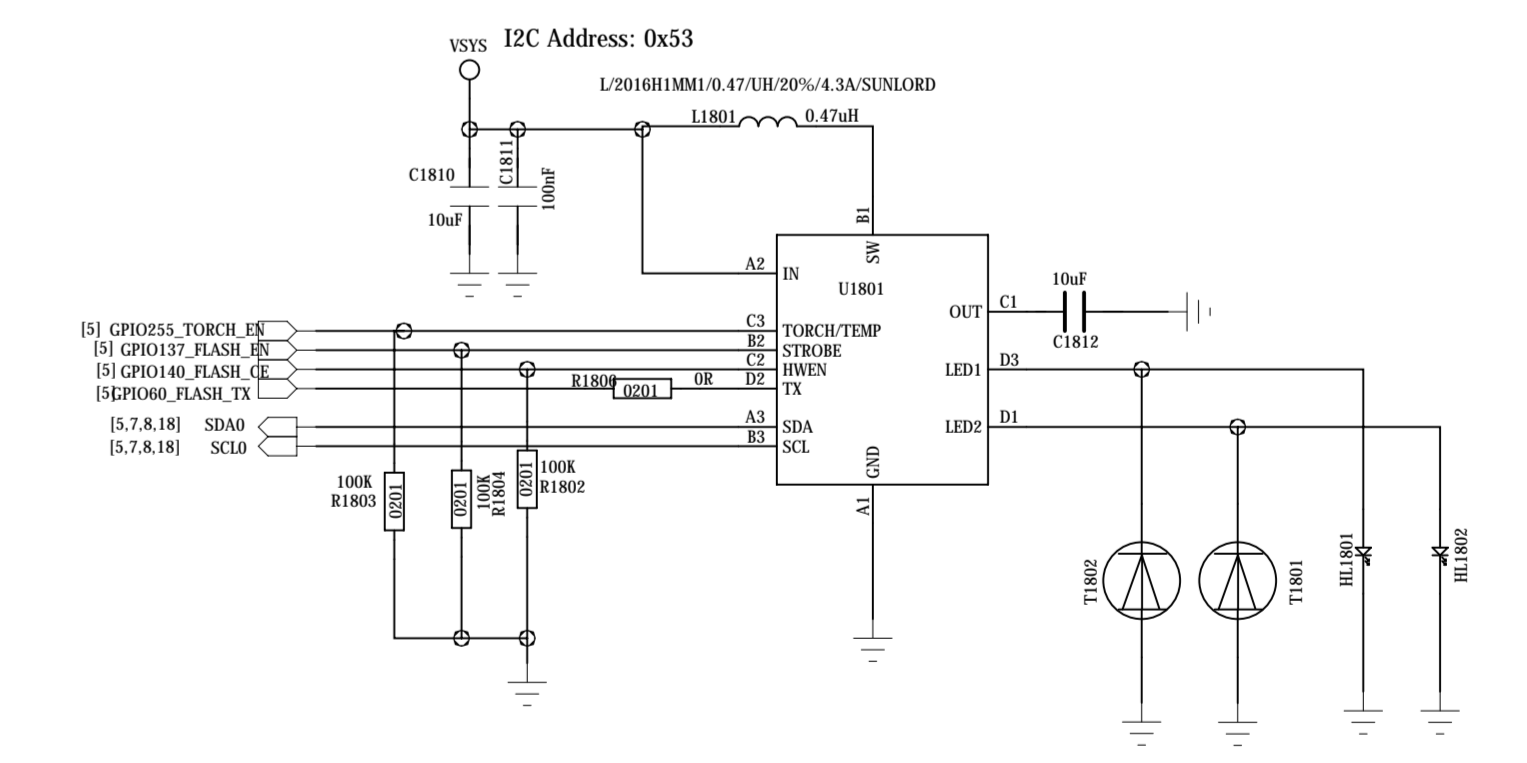
Front Camera



Black Light



Flash



Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

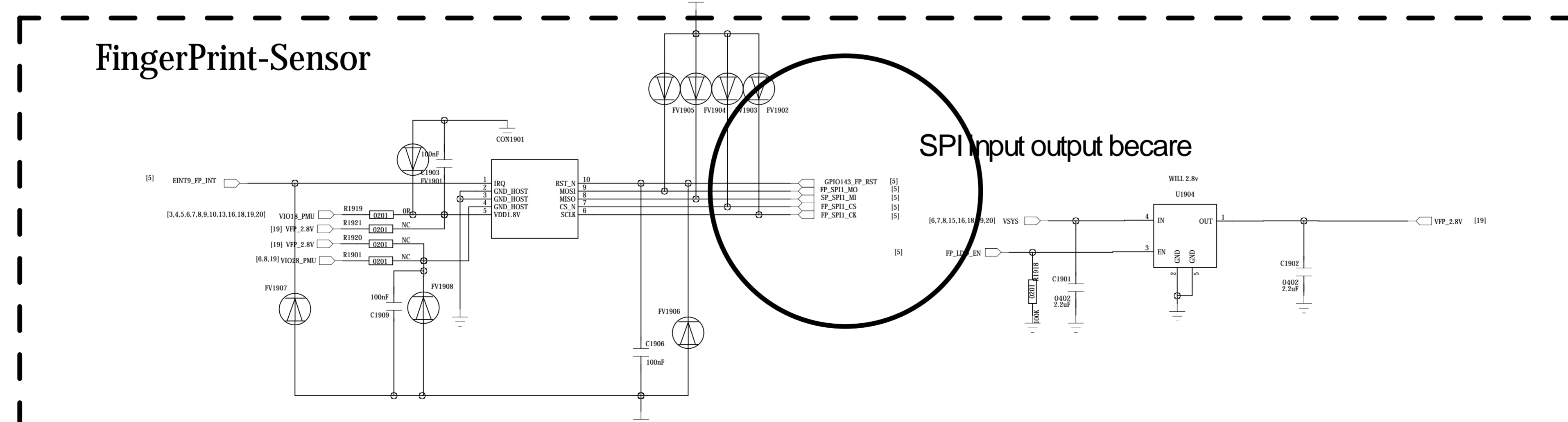
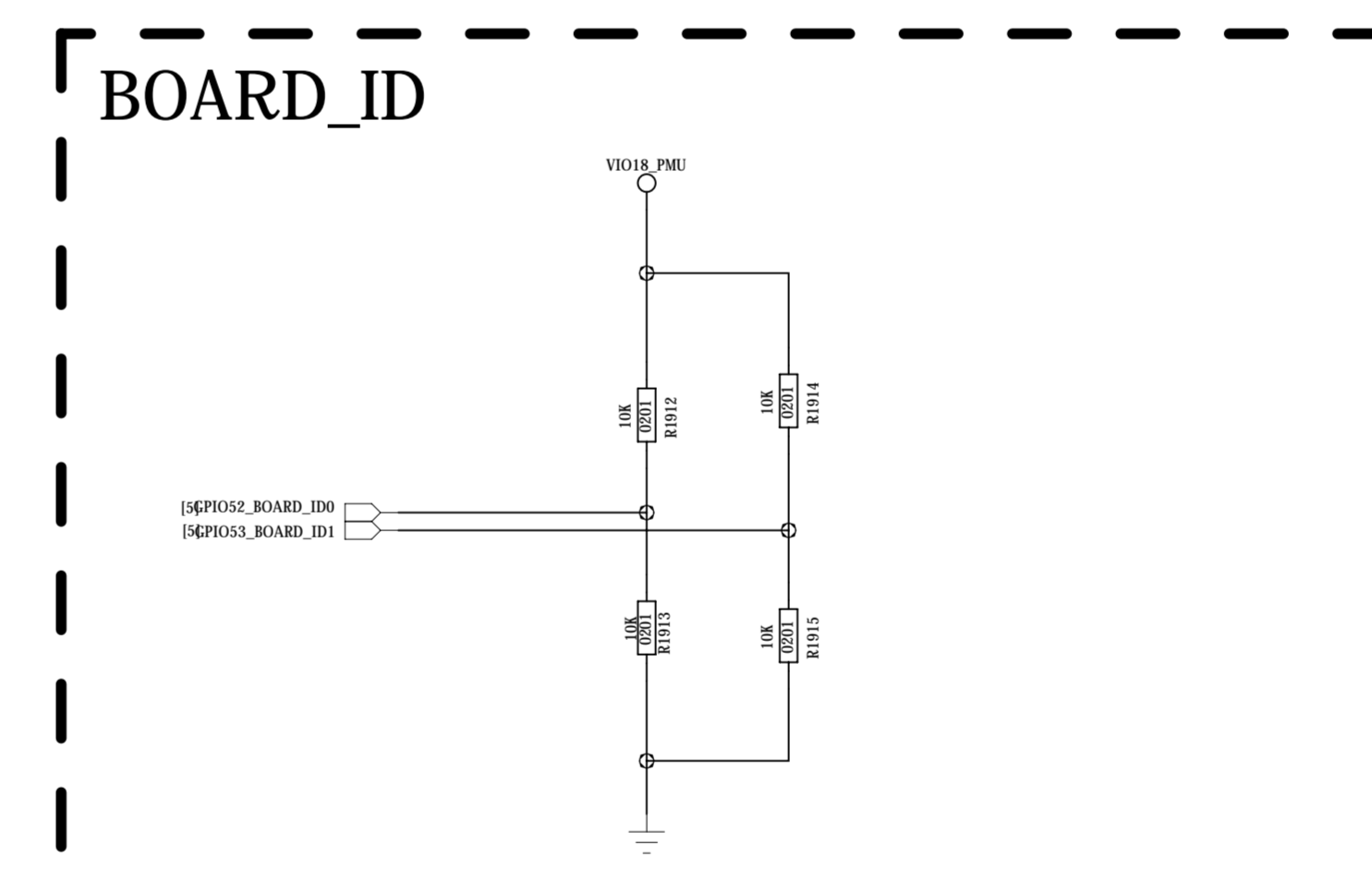
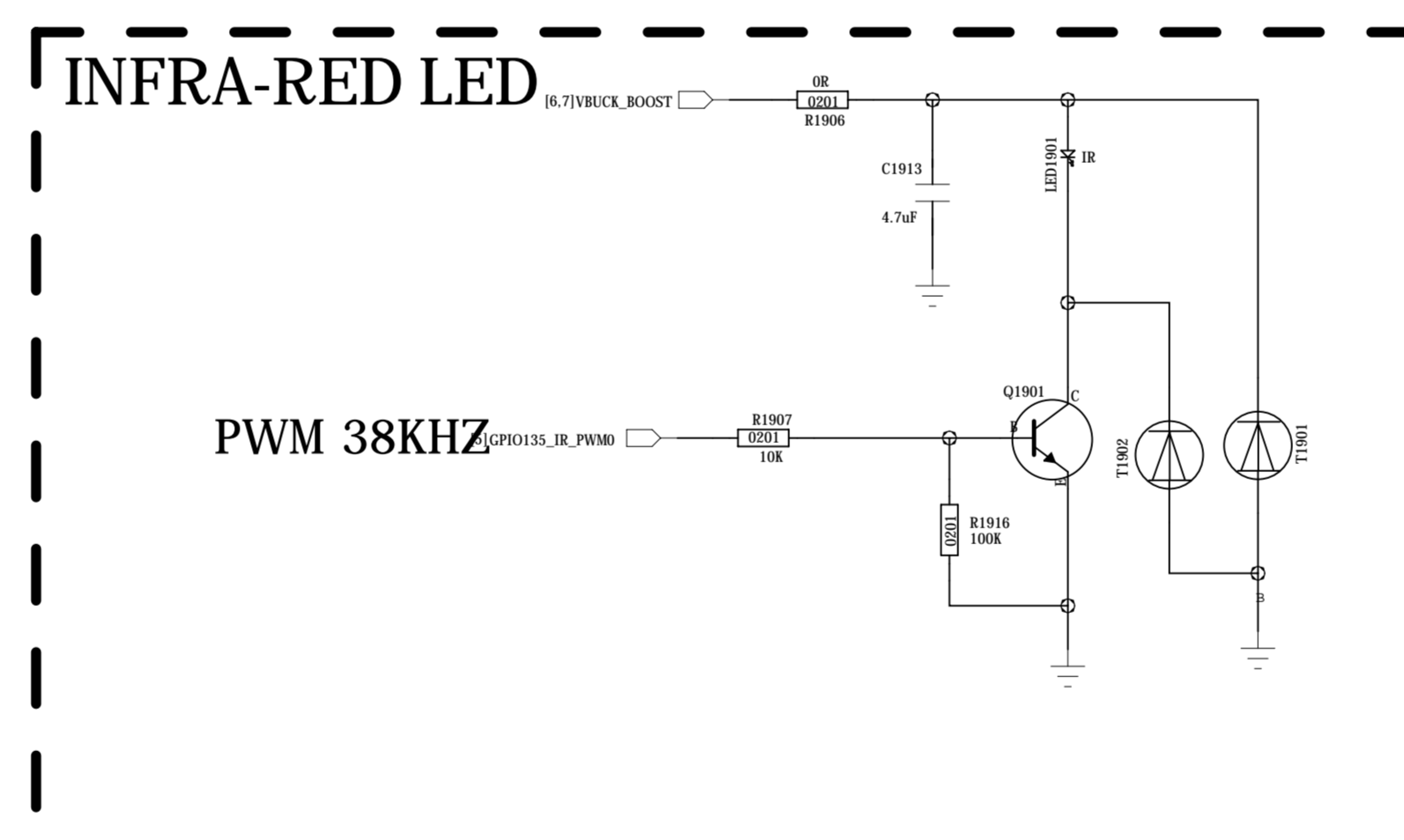
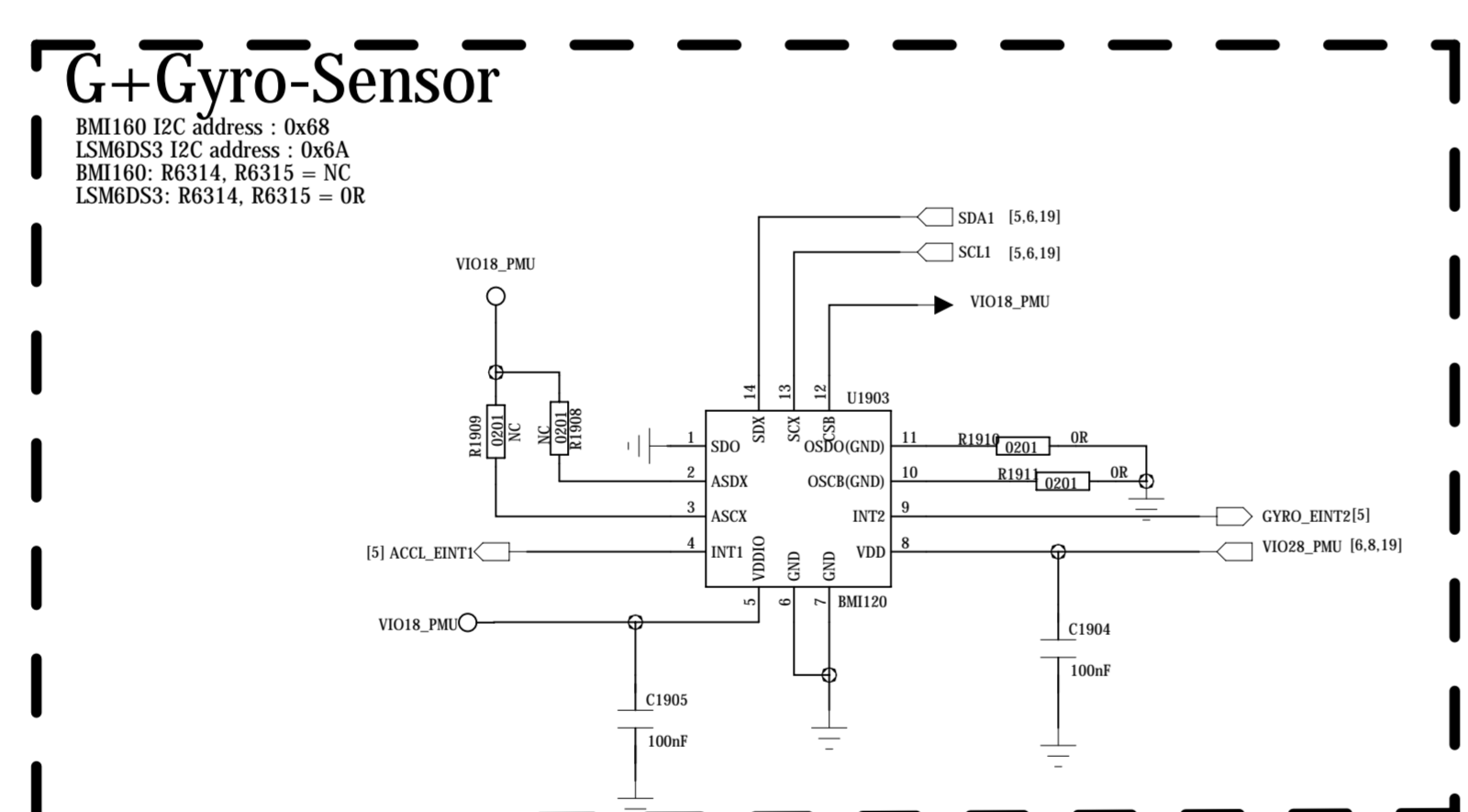
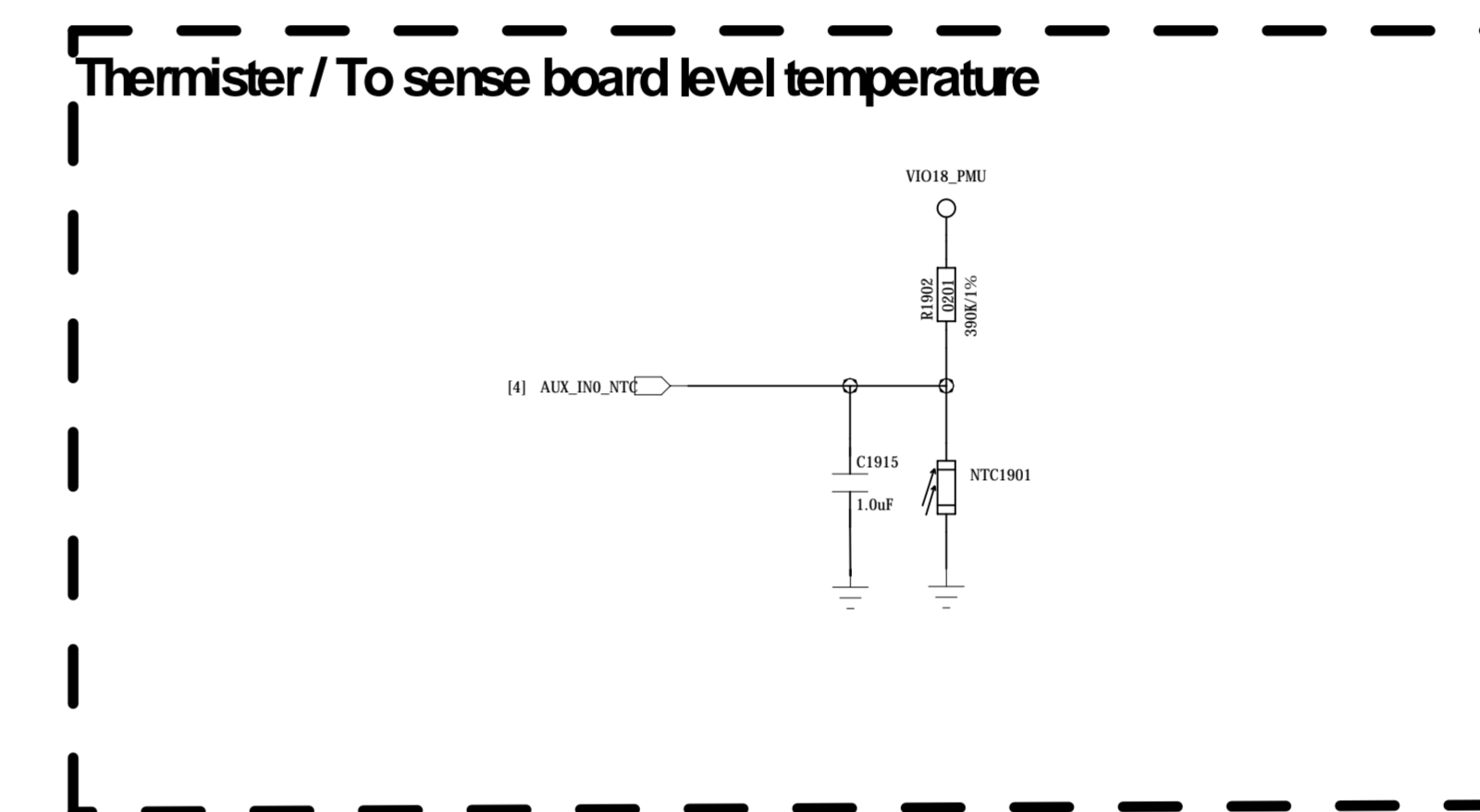
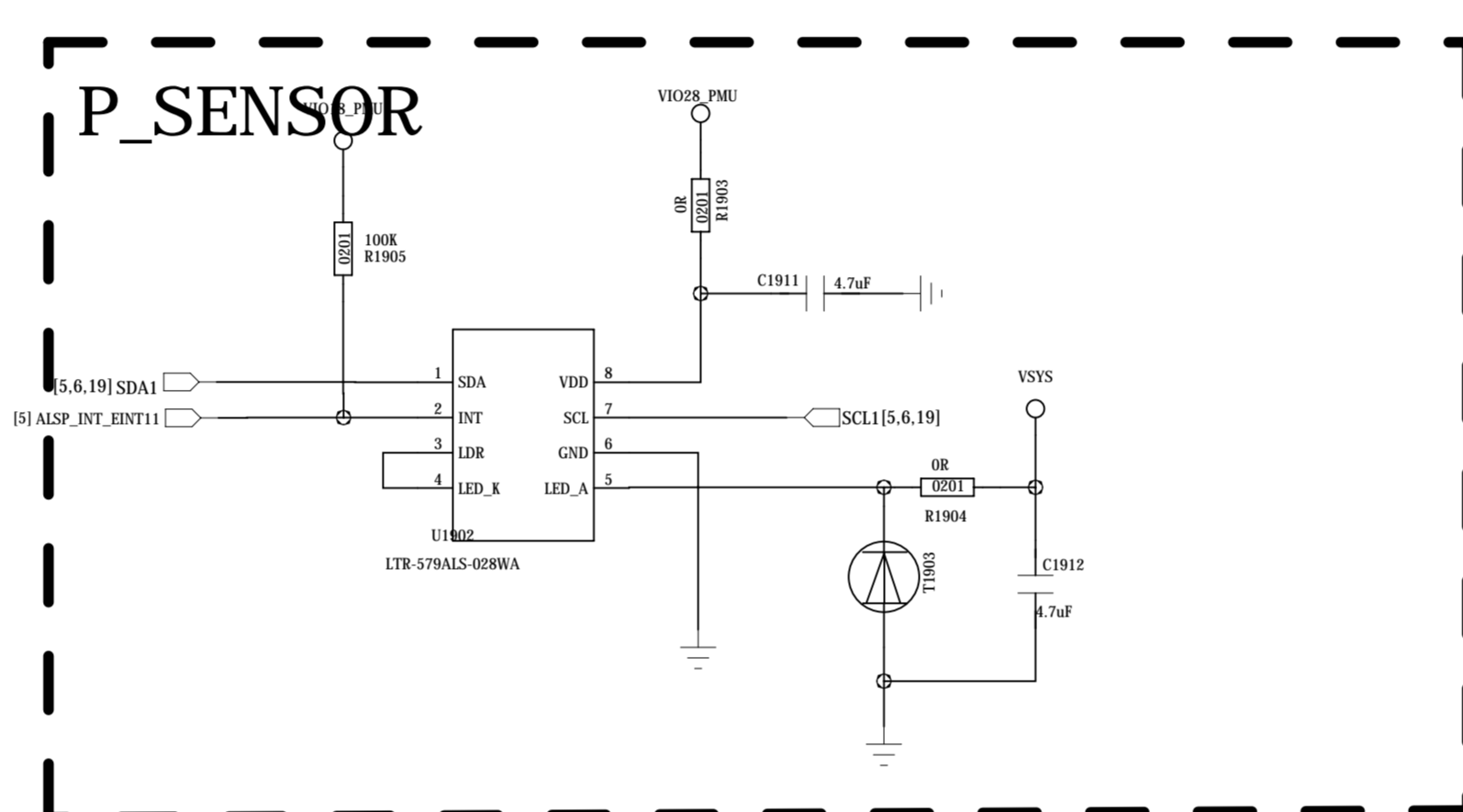
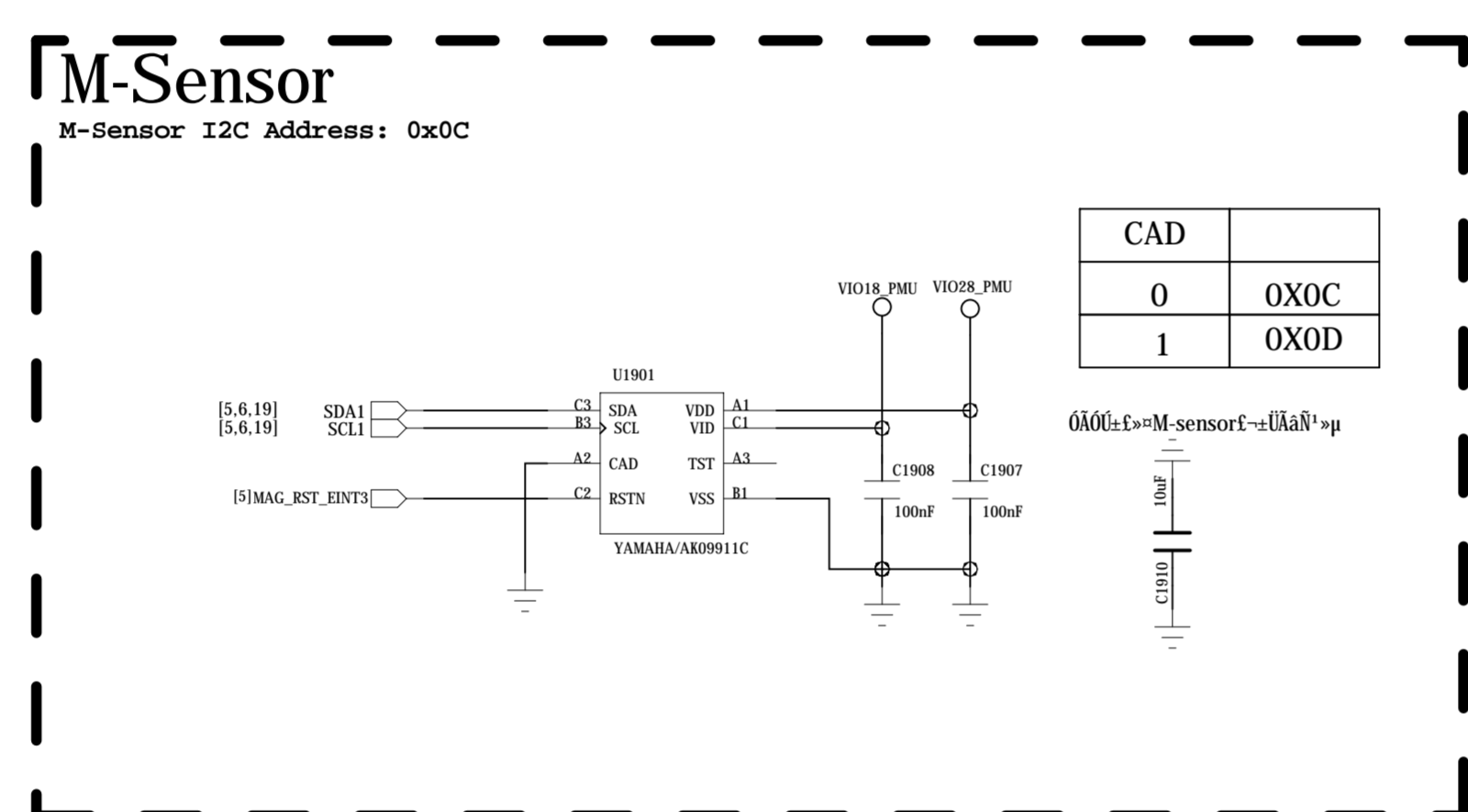
Note 62-1: The VCC of I2C_0 is pulled to "VCAM_IO_PMU".

Note 62-2: I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.

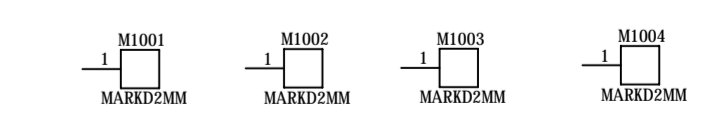
Note 62-3: Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

COMPANY		IC	
TITLE		CX880	
DRAWN: <Drawn By>	DATE: <Drawn Date>	CODE	SIZE
DESIGNED: <Checked By>	DATE: <Checked Date>	DRAWING NO.	
QUALITY CONTROL: <QC By>	DATE: <QC Date>	REV.	
RELEASED: <Released By>	DATE: <Release Date>	SCALE <Scale>	
		SHEET 48 20	

REVISION RECORD			
REV	REV NO	APPROVED	DATE

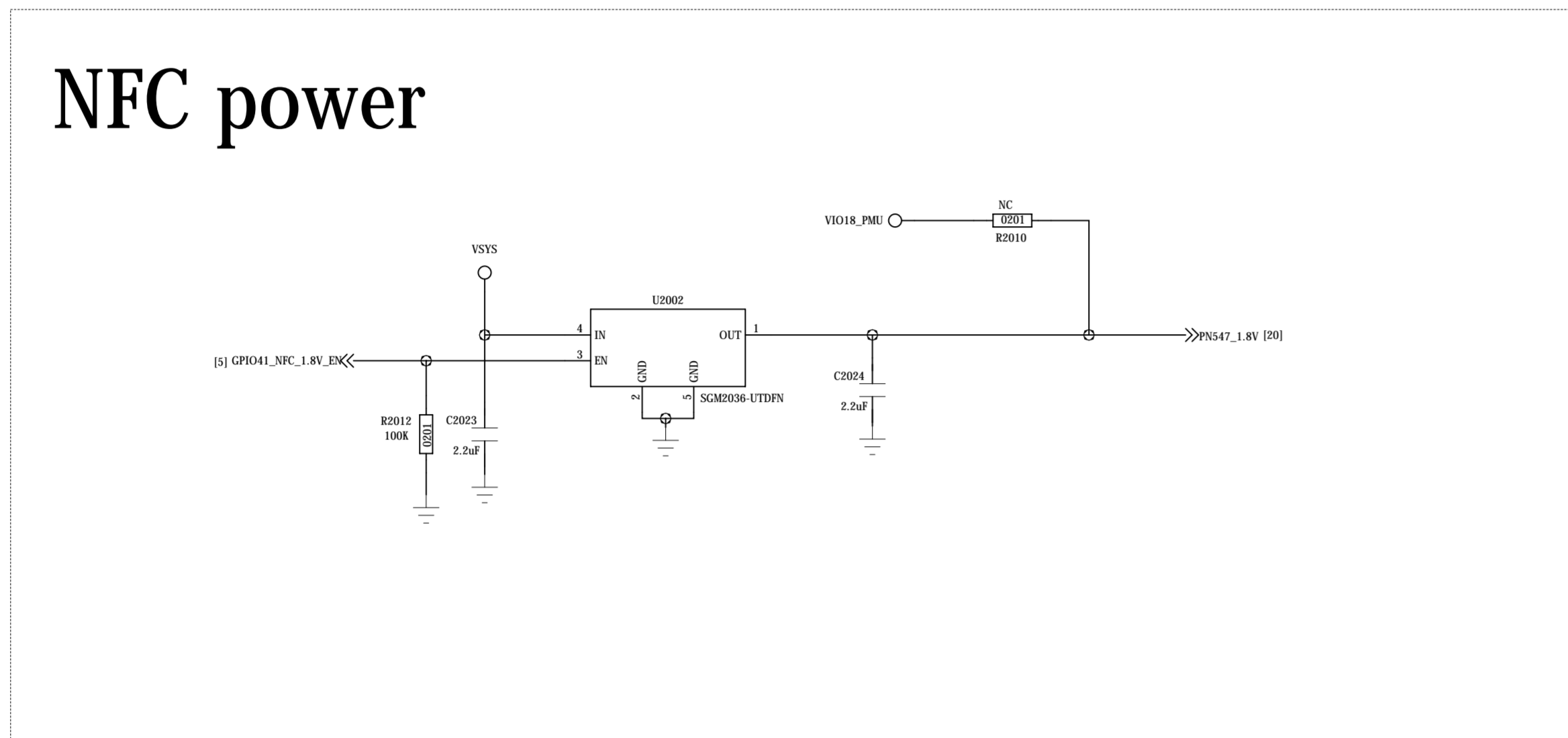
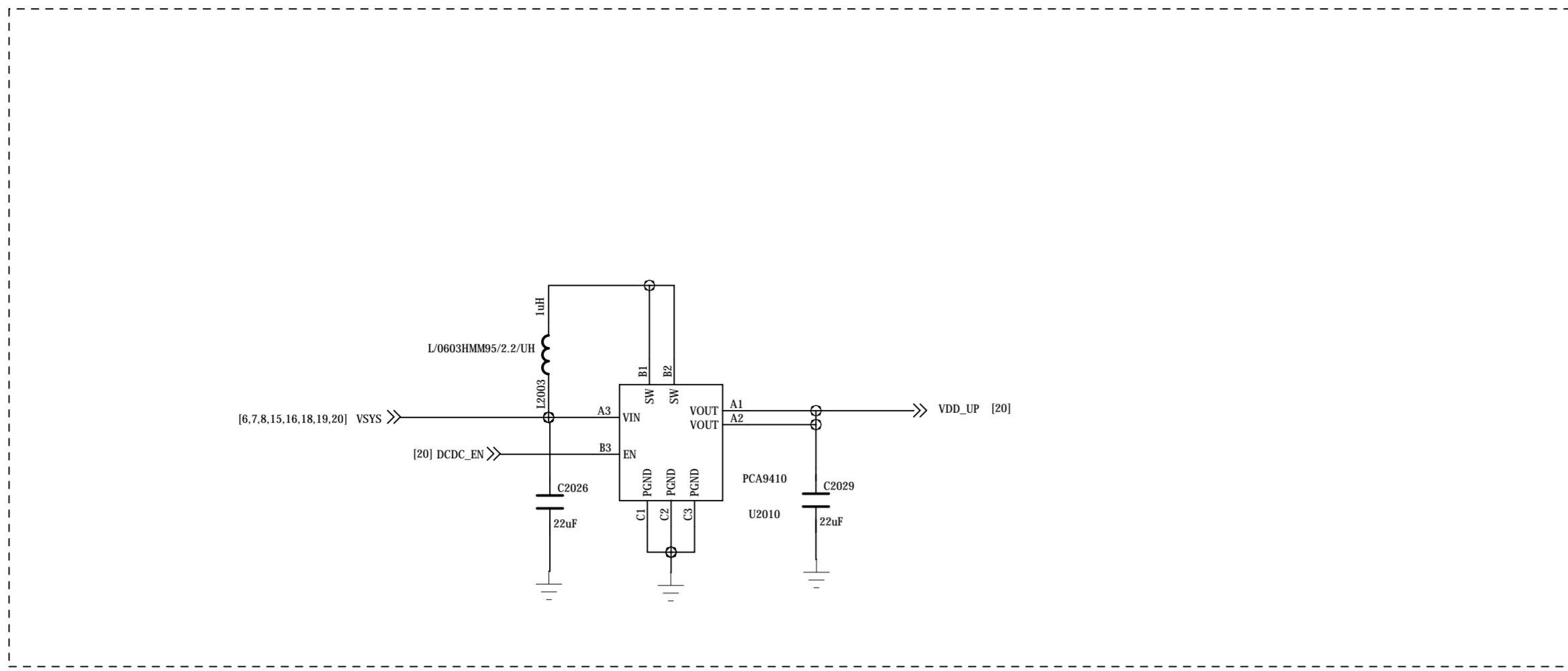


MARK POINT

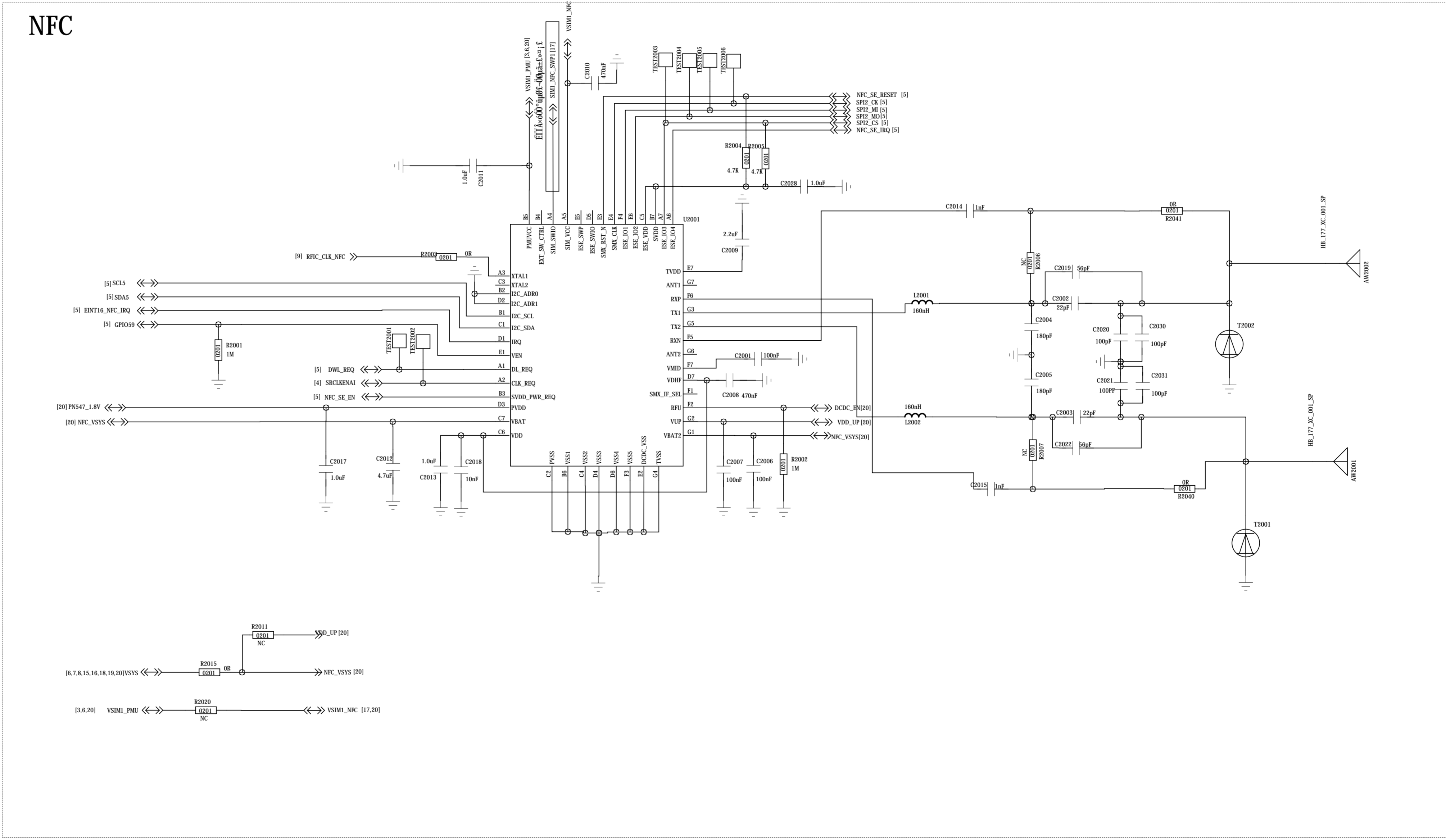


DRAWN: <Drawn By>		DATE: <Drawn Date>		COMPANY: LC	
CHECKED: <Checked By>		DATE: <Checked Date>		TITLE: CX880	
QUALITY CONTROL: <QC By>		DATE: <QC Date>		CODE: <Code>	SIZE: A0
RELEASED: <Released By>		DATE: <Release Date>		DRAWING NO: <Drawing Number>	
SCALE: <Scale>		SHEET: 10		20	

REVISION RECORD			
REV	REV NO	APPROVED	DATE



I2C_ADR1	I2C_ADR0	WRITE	READ
0	0	0X50	0X51
0	1	0X52	0X53
1	0	0X54	0X55
1	1	0X56	0X57



COMPANY		LC	
TITLE		CX880	
DRAWN	DATE	CODE	SIZE
<Drawn By>	<Drawn Date>	<Code>	A0
CHECKED	DATE	DRAWING NO.	
<Checked By>	<Checked Date>	<Drawing Number> Revision	
QUALITY CONTROL	DATE	SCALE	
<QC By>	<QC Date>	<Scale>	
RELEASED	DATE	SHEET	
<Released By>	<Release Date>	20 20	